



# **MIPS® BusBridge™ 2 Module Errata**

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# MIPS® BusBridge™ 2 Module Errata

## 1.1 Errata

Table 1.1 Summary of Errata

Erratum Number	Description	Status
E1.	After starting an AHB address phase the address and control signals are not held stable until hready is sampled high.	Fixed in Rev 2.2
E2.	VCS™ compilation fails in non-interactive mode	Fixed in Rev 2.2
E3.	MBB2 in low latency mode only - After starting an AHB address phase the address and control signals are not held stable until hready is sampled high.	Fixed in Rev 3.0

### *E1. AHB Address phase sometime not held stable*

When starting an AHB Address phase MBB2 does not hold the address and control signals stable if hready is inactive.

**Problem:** If in cycle N MBB2 is granted the bus (its hgrant signal high and hready high) it drives the address and control signals in cycle N+1 and should then keep them stable until hready is sampled high, indicating the end of the MBB2 address phase. Unfortunately this check is not performed and MBB2 will then drive its next pipelined cycle (or IDLE) onto the bus in cycle N+2.. This situation only arises when the cycle in which MBB2 is granted the bus coincides with the last address phase of the previous bus owner *and* the slave responds to this address phase by driving hready low.

**Status:** Fixed in Rev 2.2

### *E2. Compiling the MBB2 testbench fails with VCS™ in non-interactive mode*

**Problem:** When compiling the testbench a \$vcdpluson system task is encountered in the file `verif/shared/monitor.v`. For VCS™ this is illegal in non-interactive mode so compilation fails.

**Workaround:** The user can modify lines 182-183 of `monitor.v` directly as follows:

**From -**

```
//`ifdef NOT_INTERACTIVE
`ifdef ndef
```

**To -**

```
`ifdef NOT_INTERACTIVE
```

## MIPS® BusBridge™ 2 Module Errata

**Status:** Fixed in Rev 2.2

### *E3. AHB Address phase sometime not held stable (low latency mode)*

This is the same as errata [E1](#). The fix for [E1](#) in Rev 2.2 did not cover the case where MBB2™ was configured in low latency mode.

**Status:** Fixed in Rev 3.0

## Revision History

In the left hand page margins of this document you may find vertical change bars to note the location of significant changes to this document since its last release. Significant changes are defined as those which you should take note of as you use the MIPS IP. Changes to correct grammar, spelling errors or similar may or may not be noted with change bars. Change bars will be removed for changes which are more than one revision old.

Please note: Limitations on the authoring tools make it difficult to place change bars on changes to figures. Change bars on figure titles are used to denote a potential change in the figure itself. Certain parts of this document (Instruction set descriptions, EJTAG register definitions) are references to Architecture specifications, and the change bars within these sections indicate alterations since the previous version of the relevant Architecture document.

<b>Date</b>	<b>Revision</b>	<b>Description</b>
May 18, 2005	1.00	<ul style="list-style-type: none"><li>• First release with Errata E1 &amp; E2.</li></ul>
June 9, 2005	1.01	<ul style="list-style-type: none"><li>• Fixed Errata table references.</li></ul>
June 9, 2005	1.02	<ul style="list-style-type: none"><li>• Fixed some typos.</li></ul>
April 28, 2006	1.03	<ul style="list-style-type: none"><li>• Added errta E3</li><li>• Converted to RFM nB1.00</li></ul>