

MIPS® DSP ASE Instruction Set Quick Reference

- Rd, Rs, Rt — DESTINATION (Rd) AND SOURCE (Rs, Rt) REGISTERS
- Ac — ACCUMULATOR REGISTER (Ac0 – Ac3)
- C, CC — CARRY (BIT 13) AND CONDITION CODE FLAGS (BITS 24-27) IN DSPCONTROL REGISTER
- POS, SIZE — POSITION AND SIZE (SCOUNT) FIELDS IN DSPCONTROL REGISTER
- ± — SIGNED OPERAND/OPERATION OR SIGN EXTENSION
- ∅ — UNSIGNED OPERAND/OPERATION OR ZERO EXTENSION
- × — INTEGER MULTIPLICATION
- ⊙ / • — FRACTIONAL MULTIPLICATION (IMPLIED SHIFT LEFT BY 1 BIT) WITH / WITHOUT ROUNDING
- ⊙ / [] — ROUNDING AND SATURATION OPERATIONS
- L / R — LEFT / RIGHT 16-BIT PART OF A RESULT OR A REGISTER
- LL, LR, RL, RR — THE FOUR BYTES IN A 32-BIT REGISTER, FROM LEFT (MSB) TO RIGHT (LSB)
- || — BOUNDARY BETWEEN TWO OR FOUR SIMD ELEMENTS IN A REGISTER
- :: — CONCATENATION OF BIT FIELDS
- R2 — DSP ASE REVISION 2 INSTRUCTION

ARITHMETIC OPERATIONS: 8-BIT DATA

ABSQ_S.QB ^{R2}	Rd, Rs	$R_{DXY} = \llbracket R_{SXY}^{\pm} \rrbracket$	$XY \in \{LL, LR, RL, RR\}$
ADDU.QB	Rd, Rs, Rt	$R_{DXY} = R_{SXY}^{\ominus} + R_{TXY}^{\ominus}$	$XY \in \{LL, LR, RL, RR\}$
ADDU_S.QB	Rd, Rs, Rt	$R_{DXY} = \llbracket R_{SXY}^{\ominus} + R_{TXY}^{\ominus} \rrbracket$	$XY \in \{LL, LR, RL, RR\}$
ADDUH.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = (R_{SXY}^{\ominus} + R_{TXY}^{\ominus}) \ggg 1$	$XY \in \{LL, LR, RL, RR\}$
ADDUH_R.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = (R_{SXY}^{\ominus} + R_{TXY}^{\ominus} + 1^{\ominus}) \ggg 1$	$XY \in \{LL, LR, RL, RR\}$
RADDU.W.QB	Rd, Rs	$R_D = R_{S_{LL}}^{\ominus} + R_{S_{LR}}^{\ominus} + R_{S_{RL}}^{\ominus} + R_{S_{RR}}^{\ominus}$	
REPL.QB	Rd, CONST8	$R_D = \text{CONST8} \lll \text{CONST8} \lll \text{CONST8} \lll \text{CONST8}$	
REPLV.QB	Rd, Rs	$R_D = R_{S_{7,0}} \lll R_{S_{7,0}} \lll R_{S_{7,0}} \lll R_{S_{7,0}}$	
SUBU.QB	Rd, Rs, Rt	$R_{DXY} = R_{SXY}^{\ominus} - R_{TXY}^{\ominus}$	$XY \in \{LL, LR, RL, RR\}$
SUBU_S.QB	Rd, Rs, Rt	$R_{DXY} = \llbracket R_{SXY}^{\ominus} - R_{TXY}^{\ominus} \rrbracket$	$XY \in \{LL, LR, RL, RR\}$
SUBUH.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = (R_{SXY}^{\ominus} - R_{TXY}^{\ominus}) \ggg 1$	$XY \in \{LL, LR, RL, RR\}$
SUBUH_R.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = (R_{SXY}^{\ominus} - R_{TXY}^{\ominus} + 1^{\ominus}) \ggg 1$	$XY \in \{LL, LR, RL, RR\}$

SHIFT OPERATIONS: 8-BIT DATA

SHLL.QB	Rd, Rs, SHIFT3	$R_{DXY} = R_{SXY} \lll \text{SHIFT3}$	$XY \in \{LL, LR, RL, RR\}$
SHLLV.QB	Rd, Rs, Rt	$R_{DXY} = R_{SXY} \lll R_{T_{2,0}}$	$XY \in \{LL, LR, RL, RR\}$
SHRA.QB ^{R2}	Rd, Rs, SHIFT3	$R_{DXY} = R_{SXY}^{\pm} \ggg \text{SHIFT3}$	$XY \in \{LL, LR, RL, RR\}$
SHRA_R.QB ^{R2}	Rd, Rs, SHIFT3	$R_{DXY} = \text{\textcircled{R}}(R_{SXY}^{\pm} \ggg \text{SHIFT3})$	$XY \in \{LL, LR, RL, RR\}$
SHRAV.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = R_{SXY}^{\pm} \ggg R_{T_{2,0}}$	$XY \in \{LL, LR, RL, RR\}$
SHRAV_R.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = \text{\textcircled{R}}(R_{SXY}^{\pm} \ggg R_{T_{2,0}})$	$XY \in \{LL, LR, RL, RR\}$
SHRL.QB	Rd, Rs, SHIFT3	$R_{DXY} = R_{SXY}^{\ominus} \ggg \text{SHIFT3}$	$XY \in \{LL, LR, RL, RR\}$
SHRLV.QB	Rd, Rs, Rt	$R_{DXY} = R_{SXY}^{\ominus} \ggg R_{T_{2,0}}$	$XY \in \{LL, LR, RL, RR\}$

UNSIGNED INTEGER MULTIPLY OPERATIONS: 8-BIT/16-BIT DATA » GPR

MULEU_S.PH.QBL	Rd, Rs, Rt	$R_D = \llbracket R_{S_{LL}}^{\ominus} \times R_{T_{LL}}^{\ominus} \rrbracket \lll \llbracket R_{S_{LR}}^{\ominus} \times R_{T_{LR}}^{\ominus} \rrbracket$	
MULEU_S.PH.QBR	Rd, Rs, Rt	$R_D = \llbracket R_{S_{RL}}^{\ominus} \times R_{T_{RL}}^{\ominus} \rrbracket \lll \llbracket R_{S_{RR}}^{\ominus} \times R_{T_{RR}}^{\ominus} \rrbracket$	

UNSIGNED INTEGER MULTIPLY OPERATIONS: 8-BIT DATA » ACCUMULATOR

DPAU.H.QBL	Ac, Rs, Rt	$Ac += (R_{S_{LL}}^{\ominus} \times R_{T_{LL}}^{\ominus}) + (R_{S_{LR}}^{\ominus} \times R_{T_{LR}}^{\ominus})$	
DPAU.H.QBR	Ac, Rs, Rt	$Ac += (R_{S_{RL}}^{\ominus} \times R_{T_{RL}}^{\ominus}) + (R_{S_{RR}}^{\ominus} \times R_{T_{RR}}^{\ominus})$	
DPSU.H.QBL	Ac, Rs, Rt	$Ac -= (R_{S_{LL}}^{\ominus} \times R_{T_{LL}}^{\ominus}) + (R_{S_{LR}}^{\ominus} \times R_{T_{LR}}^{\ominus})$	
DPSU.H.QBR	Ac, Rs, Rt	$Ac -= (R_{S_{RL}}^{\ominus} \times R_{T_{RL}}^{\ominus}) + (R_{S_{RR}}^{\ominus} \times R_{T_{RR}}^{\ominus})$	

PRECISION EXPANSION (DATA UNPACKING) OPERATIONS: 8-BIT DATA

PRECEQU.PH.QBL	Rd, Rs	$R_D = (R_{S_{LL}} \lll 7) \lll (R_{S_{LR}} \lll 7)$	
PRECEQU.PH.QBLA	Rd, Rs	$R_D = (R_{S_{LL}} \lll 7) \lll (R_{S_{RL}} \lll 7)$	
PRECEQU.PH.QBR	Rd, Rs	$R_D = (R_{S_{RL}} \lll 7) \lll (R_{S_{RR}} \lll 7)$	
PRECEQU.PH.QBRA	Rd, Rs	$R_D = (R_{S_{LR}} \lll 7) \lll (R_{S_{RR}} \lll 7)$	
PRECEU.PH.QBL	Rd, Rs	$R_D = 0^8 \lll R_{S_{LL}} \lll 0^8 \lll R_{S_{LR}}$	
PRECEU.PH.QBLA	Rd, Rs	$R_D = 0^8 \lll R_{S_{LL}} \lll 0^8 \lll R_{S_{RL}}$	
PRECEU.PH.QBR	Rd, Rs	$R_D = 0^8 \lll R_{S_{RL}} \lll 0^8 \lll R_{S_{RR}}$	
PRECEU.PH.QBRA	Rd, Rs	$R_D = 0^8 \lll R_{S_{LR}} \lll 0^8 \lll R_{S_{RR}}$	

COMPARE AND PICK OPERATIONS: 8-BIT DATA

CMPGDU.EQ.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = CC_{XY} = (R_{SXY}^{\ominus} = R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
CMPGDU.LT.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = CC_{XY} = (R_{SXY}^{\ominus} < R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
CMPGDU.LE.QB ^{R2}	Rd, Rs, Rt	$R_{DXY} = CC_{XY} = (R_{SXY}^{\ominus} \leq R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
CMPGU.EQ.QB	Rd, Rs, Rt	$R_{DXY} = (R_{SXY}^{\ominus} = R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
CMPGU.LT.QB	Rd, Rs, Rt	$R_{DXY} = (R_{SXY}^{\ominus} < R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
CMPGU.LE.QB	Rd, Rs, Rt	$R_{DXY} = (R_{SXY}^{\ominus} \leq R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
CMPU.EQ.QB	Rd, Rs, Rt	$CC_{XY} = (R_{SXY}^{\ominus} = R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
CMPU.LT.QB	Rd, Rs, Rt	$CC_{XY} = (R_{SXY}^{\ominus} < R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
CMPU.LE.QB	Rd, Rs, Rt	$CC_{XY} = (R_{SXY}^{\ominus} \leq R_{TXY}^{\ominus}) ? 1 : 0$	$XY \in \{LL, LR, RL, RR\}$
PICK.QB	Rd, Rs, Rt	$R_{DXY} = CC_{XY} ? R_{SXY} : R_{TXY}$	$XY \in \{LL, LR, RL, RR\}$

COMPARE AND PICK OPERATIONS: 16-BIT DATA

CMP.EQ.PH	Rd, Rs, Rt	$CC = ((R_{S_L}^{\pm} = R_{T_L}^{\pm}) ? 1 : 0) \lll ((R_{S_R}^{\pm} = R_{T_R}^{\pm}) ? 1 : 0)$
CMP.LT.PH	Rd, Rs, Rt	$CC = ((R_{S_L}^{\pm} < R_{T_L}^{\pm}) ? 1 : 0) \lll ((R_{S_R}^{\pm} < R_{T_R}^{\pm}) ? 1 : 0)$
CMP.LE.PH	Rd, Rs, Rt	$CC = ((R_{S_L}^{\pm} \leq R_{T_L}^{\pm}) ? 1 : 0) \lll ((R_{S_R}^{\pm} \leq R_{T_R}^{\pm}) ? 1 : 0)$
PICK.PH	Rd, Rs, Rt	$R_D = (CC_L ? R_{S_L} : R_{T_L}) \lll (CC_R ? R_{S_R} : R_{T_R})$



ARITHMETIC OPERATIONS: 16-BIT DATA		
ABSQ_S.PH	R _D , R _S	$R_D = [R_{S_L}^{\pm}] \parallel [R_{S_R}^{\pm}]$
ADDQ.PH	R _D , R _S , R _T	$R_D = (R_{S_L}^{\pm} + R_{T_L}^{\pm}) \parallel (R_{S_R}^{\pm} + R_{T_R}^{\pm})$
ADDQ_S.PH	R _D , R _S , R _T	$R_D = [R_{S_L}^{\pm} + R_{T_L}^{\pm}] \parallel [R_{S_R}^{\pm} + R_{T_R}^{\pm}]$
ADDQH.PH ^{R2}	R _D , R _S , R _T	$R_D = ((R_{S_L}^{\pm} + R_{T_L}^{\pm}) \gg 1) \parallel ((R_{S_R}^{\pm} + R_{T_R}^{\pm}) \gg 1)$
ADDQH_R.PH ^{R2}	R _D , R _S , R _T	$R_D = @((R_{S_L}^{\pm} + R_{T_L}^{\pm}) \gg 1) \parallel @((R_{S_R}^{\pm} + R_{T_R}^{\pm}) \gg 1)$
ADDU.PH ^{R2}	R _D , R _S , R _T	$R_D = (R_{S_L}^{\circ} + R_{T_L}^{\circ}) \parallel (R_{S_R}^{\circ} + R_{T_R}^{\circ})$
ADDU_S.PH ^{R2}	R _D , R _S , R _T	$R_D = [R_{S_L}^{\circ} + R_{T_L}^{\circ}] \parallel [R_{S_R}^{\circ} + R_{T_R}^{\circ}]$
REPL.PH	R _D , CONST10	$R_D = \text{CONST10}^{\pm} \parallel \text{CONST10}^{\pm}$
REPLV.PH	R _D , R _S	$R_D = R_{S_{15:0}} \parallel R_{S_{15:0}}$
SUBQ.PH	R _D , R _S , R _T	$R_D = (R_{S_L}^{\pm} - R_{T_L}^{\pm}) \parallel (R_{S_R}^{\pm} - R_{T_R}^{\pm})$
SUBQ_S.PH	R _D , R _S , R _T	$R_D = [R_{S_L}^{\pm} - R_{T_L}^{\pm}] \parallel [R_{S_R}^{\pm} - R_{T_R}^{\pm}]$
SUBQH.PH ^{R2}	R _D , R _S , R _T	$R_D = ((R_{S_L}^{\pm} - R_{T_L}^{\pm}) \gg 1) \parallel ((R_{S_R}^{\pm} - R_{T_R}^{\pm}) \gg 1)$
SUBQH_R.PH ^{R2}	R _D , R _S , R _T	$R_D = @((R_{S_L}^{\pm} - R_{T_L}^{\pm}) \gg 1) \parallel @((R_{S_R}^{\pm} - R_{T_R}^{\pm}) \gg 1)$
SUBU.PH ^{R2}	R _D , R _S , R _T	$R_D = (R_{S_L}^{\circ} - R_{T_L}^{\circ}) \parallel (R_{S_R}^{\circ} - R_{T_R}^{\circ})$
SUBU_S.PH ^{R2}	R _D , R _S , R _T	$R_D = [R_{S_L}^{\circ} - R_{T_L}^{\circ}] \parallel [R_{S_R}^{\circ} - R_{T_R}^{\circ}]$

SHIFT OPERATIONS: 16-BIT DATA		
SHLL.PH	R _D , R _S , SHIFT4	$R_D = (R_{S_L} \ll \text{SHIFT4}) \parallel (R_{S_R} \ll \text{SHIFT4})$
SHLL_S.PH	R _D , R _S , SHIFT4	$R_D = [R_{S_L} \ll \text{SHIFT4}] \parallel [R_{S_R} \ll \text{SHIFT4}]$
SHLLV.PH	R _D , R _S , R _T	$R_D = (R_{S_L} \ll R_{T_{3:0}}) \parallel (R_{S_R} \ll R_{T_{3:0}})$
SHLLV_S.PH	R _D , R _S , R _T	$R_D = [R_{S_L} \ll R_{T_{3:0}}] \parallel [R_{S_R} \ll R_{T_{3:0}}]$
SHRA.PH	R _D , R _S , SHIFT4	$R_D = (R_{S_L}^{\pm} \gg \text{SHIFT4}) \parallel (R_{S_R}^{\pm} \gg \text{SHIFT4})$
SHRA_R.PH	R _D , R _S , SHIFT4	$R_D = @((R_{S_L}^{\pm} \gg \text{SHIFT4}) \parallel @((R_{S_R}^{\pm} \gg \text{SHIFT4}))$
SHRAV.PH	R _D , R _S , R _T	$R_D = (R_{S_L}^{\pm} \gg R_{T_{3:0}}) \parallel (R_{S_R}^{\pm} \gg R_{T_{3:0}})$
SHRAV_R.PH	R _D , R _S , R _T	$R_D = @((R_{S_L}^{\pm} \gg R_{T_{3:0}}) \parallel @((R_{S_R}^{\pm} \gg R_{T_{3:0}}))$
SHRL.PH ^{R2}	R _D , R _S , SHIFT4	$R_D = (R_{S_L}^{\circ} \gg \text{SHIFT4}) \parallel (R_{S_R}^{\circ} \gg \text{SHIFT4})$
SHRLV.PH ^{R2}	R _D , R _S , R _T	$R_D = (R_{S_L}^{\circ} \gg R_{T_{3:0}}) \parallel (R_{S_R}^{\circ} \gg R_{T_{3:0}})$

PRECISION REDUCTION (DATA PACKING) OPERATIONS: 16-BIT DATA		
PRECR.QB.PH ^{R2}	R _D , R _S , R _T	$R_D = R_{S_{LR}} \parallel R_{S_{RR}} \parallel R_{T_{LR}} \parallel R_{T_{RR}}$
PRECRQ.QB.PH	R _D , R _S , R _T	$R_D = R_{S_{LL}} \parallel R_{S_{RL}} \parallel R_{T_{LL}} \parallel R_{T_{RL}}$
PRECRQU_S.QB.PH	R _D , R _S , R _T	$R_D = [R_{S_L}^{\circ}]_{14:7} \parallel [R_{S_R}^{\circ}]_{14:7} \parallel [R_{T_L}^{\circ}]_{14:7} \parallel [R_{T_R}^{\circ}]_{14:7}$

PRECISION EXPANSION (DATA UNPACKING) OPERATIONS: 16-BIT DATA		
PRECEQ.W.PHL	R _D , R _S	$R_D = R_{S_L} \ll 16$
PRECEQ.W.PHR	R _D , R _S	$R_D = R_{S_R} \ll 16$

INTEGER MULTIPLY OPERATIONS: 16-BIT DATA » ACCUMULATOR		
DPA.W.PH ^{R2}	Ac, R _S , R _T	$Ac += (R_{S_L}^{\pm} \times R_{T_L}^{\pm}) + (R_{S_R}^{\pm} \times R_{T_R}^{\pm})$
DPAX.W.PH ^{R2}	Ac, R _S , R _T	$Ac += (R_{S_L}^{\pm} \times R_{T_R}^{\pm}) + (R_{S_R}^{\pm} \times R_{T_L}^{\pm})$
DPS.W.PH ^{R2}	Ac, R _S , R _T	$Ac -= (R_{S_L}^{\pm} \times R_{T_L}^{\pm}) + (R_{S_R}^{\pm} \times R_{T_R}^{\pm})$
DPSX.W.PH ^{R2}	Ac, R _S , R _T	$Ac -= (R_{S_L}^{\pm} \times R_{T_R}^{\pm}) + (R_{S_R}^{\pm} \times R_{T_L}^{\pm})$
MULSA.W.PH ^{R2}	Ac, R _S , R _T	$Ac += (R_{S_L}^{\pm} \times R_{T_L}^{\pm}) - (R_{S_R}^{\pm} \times R_{T_R}^{\pm})$

INTEGER MULTIPLY OPERATIONS: 16-BIT DATA » GPR		
MUL.PH ^{R2}	R _D , R _S , R _T	$R_D = (R_{S_L}^{\pm} \times R_{T_L}^{\pm})_R \parallel (R_{S_R}^{\pm} \times R_{T_R}^{\pm})_R$
MUL_S.PH ^{R2}	R _D , R _S , R _T	$R_D = [R_{S_L}^{\pm} \times R_{T_L}^{\pm}]_R \parallel [R_{S_R}^{\pm} \times R_{T_R}^{\pm}]_R$

FRACTIONAL MULTIPLY OPERATIONS: 16-BIT DATA » GPR		
MULQ_RS.PH	R _D , R _S , R _T	$R_D = [R_{S_L}^{\pm} \odot R_{T_L}^{\pm}]_L \parallel [R_{S_R}^{\pm} \odot R_{T_R}^{\pm}]_L$
MULQ_S.PH ^{R2}	R _D , R _S , R _T	$R_D = [R_{S_L}^{\pm} \bullet R_{T_L}^{\pm}]_L \parallel [R_{S_R}^{\pm} \bullet R_{T_R}^{\pm}]_L$
MULEQ_S.W.PHL	R _D , R _S , R _T	$R_D = [R_{S_L}^{\pm} \bullet R_{T_L}^{\pm}]$
MULEQ_S.W.PHR	R _D , R _S , R _T	$R_D = [R_{S_R}^{\pm} \bullet R_{T_R}^{\pm}]$

FRACTIONAL MULTIPLY OPERATIONS: 16-BIT DATA » ACCUMULATOR		
DPAQ_S.W.PH	Ac, R _S , R _T	$Ac += [R_{S_L}^{\pm} \bullet R_{T_L}^{\pm}] + [R_{S_R}^{\pm} \bullet R_{T_R}^{\pm}]$
DPAQX_S.W.PH ^{R2}	Ac, R _S , R _T	$Ac += [R_{S_L}^{\pm} \bullet R_{T_R}^{\pm}] + [R_{S_R}^{\pm} \bullet R_{T_L}^{\pm}]$
DPAQX_SA.W.PH ^{R2}	Ac, R _S , R _T	$Ac = [Ac + [R_{S_L}^{\pm} \bullet R_{T_R}^{\pm}] + [R_{S_R}^{\pm} \bullet R_{T_L}^{\pm}]]$
DPSQ_S.W.PH	Ac, R _S , R _T	$Ac -= [R_{S_L}^{\pm} \bullet R_{T_L}^{\pm}] + [R_{S_R}^{\pm} \bullet R_{T_R}^{\pm}]$
DPSQX_S.W.PH ^{R2}	Ac, R _S , R _T	$Ac -= [R_{S_L}^{\pm} \bullet R_{T_R}^{\pm}] + [R_{S_R}^{\pm} \bullet R_{T_L}^{\pm}]$
DPSQX_SA.W.PH ^{R2}	Ac, R _S , R _T	$Ac = [Ac - [R_{S_L}^{\pm} \bullet R_{T_R}^{\pm}] + [R_{S_R}^{\pm} \bullet R_{T_L}^{\pm}]]$
MULSAQ_S.W.PH	Ac, R _S , R _T	$Ac += [R_{S_L}^{\pm} \bullet R_{T_L}^{\pm}] - [R_{S_R}^{\pm} \bullet R_{T_R}^{\pm}]$
MAQ_S.W.PHL	Ac, R _S , R _T	$Ac += [R_{S_L}^{\pm} \bullet R_{T_L}^{\pm}]$
MAQ_S.W.PHR	Ac, R _S , R _T	$Ac += [R_{S_R}^{\pm} \bullet R_{T_R}^{\pm}]$
MAQ_SA.W.PHL	Ac, R _S , R _T	$Ac = [Ac^+ + [R_{S_L}^{\pm} \bullet R_{T_L}^{\pm}]]$
MAQ_SA.W.PHR	Ac, R _S , R _T	$Ac = [Ac^+ + [R_{S_R}^{\pm} \bullet R_{T_R}^{\pm}]]$

ACCUMULATOR EXTRACT OPERATIONS: 16-BIT DATA		
EXTR_S.H	R _D , Ac, SHIFT5	$R_D = [Ac \gg \text{SHIFT5}]_R$
EXTRV_S.H	R _D , Ac, R _T	$R_D = [Ac \gg R_{T_{4:0}}]_R$

DSP CONTROL REGISTER ACCESS OPERATIONS		
RDDSP	R _D , MASK10	$R_D = \text{READDSPCONTROL}(\text{MASK10}_{5:0})$
WRDSP	R _S , MASK10	$\text{WRITEDSPCONTROL}(\text{MASK10}_{5:0}, R_S)$



ARITHMETIC OPERATIONS: 32-BIT DATA		
ABSQ_S.W	Rd, Rs	$R_D = [R_S]$
ADDQ_S.W	Rd, Rs, Rt	$R_D = [R_S^{\pm} + R_T^{\pm}]$
ADDQH.W ^{R2}	Rd, Rs, Rt	$R_D = (R_S^{\pm} + R_T^{\pm}) \gg 1$
ADDQH_R.W ^{R2}	Rd, Rs, Rt	$R_D = @((R_S^{\pm} + R_T^{\pm}) \gg 1)$
ADDSC	Rd, Rs, Rt	$C::R_D = R_S^{\circ} + R_T^{\circ}$
ADDWC	Rd, Rs, Rt	$R_D = R_S^{\circ} + R_T^{\circ} + C$
SUBQ_S.W	Rd, Rs, Rt	$R_D = [R_S - R_T]$
SUBQH.W ^{R2}	Rd, Rs, Rt	$R_D = (R_S^{\pm} - R_T^{\pm}) \gg 1$
SUBQH_R.W ^{R2}	Rd, Rs, Rt	$R_D = @((R_S^{\pm} - R_T^{\pm}) \gg 1)$

SHIFT OPERATIONS: 32-BIT DATA		
SHLL_S.W	Rd, Rs, SHIFT5	$R_D = [R_S \ll \text{SHIFT}5]$
SHLLV_S.W	Rd, Rs, Rt	$R_D = [R_S \ll R_{T40}]$
SHRA_R.W	Rd, Rs, SHIFT5	$R_D = @([R_S^{\pm} \gg \text{SHIFT}5])$
SHRAV_R.W	Rd, Rs, Rt	$R_D = @[R_S^{\pm} \gg R_{T40}]$

FRACTIONAL MULTIPLY OPERATIONS: 32-BIT DATA » GPR		
MULQ_RS.W ^{R2}	Rd, Rs, Rt	$R_D = [R_S^{\pm} \odot R_T^{\pm}]_L$
MULQ_S.W ^{R2}	Rd, Rs, Rt	$R_D = [R_S^{\pm} \bullet R_T^{\pm}]_L$

FRACTIONAL MULTIPLY OPERATIONS: 32-BIT DATA » ACCUMULATOR		
DPAQ_SA.L.W	Ac, Rs, Rt	$Ac = [Ac^{\pm} + [R_S^{\pm} \bullet R_T^{\pm}]]$
DPSQ_SA.L.W	Ac, Rs, Rt	$Ac = [Ac^{\pm} - [R_S^{\pm} \bullet R_T^{\pm}]]$

INTEGER MULTIPLY OPERATIONS: 32-BIT DATA » ACCUMULATOR		
MADD ^{R2}	Ac, Rs, Rt	$Ac += R_S^{\pm} \times R_T^{\pm}$
MADDU ^{R2}	Ac, Rs, Rt	$Ac += R_S^{\circ} \times R_T^{\circ}$
MSUB ^{R2}	Ac, Rs, Rt	$Ac -= R_S^{\pm} \times R_T^{\pm}$
MSUBU ^{R2}	Ac, Rs, Rt	$Ac -= R_S^{\circ} \times R_T^{\circ}$
MULT ^{R2}	Ac, Rs, Rt	$Ac = R_S^{\pm} \times R_T^{\pm}$
MULTU ^{R2}	Ac, Rs, Rt	$Ac = R_S^{\circ} \times R_T^{\circ}$

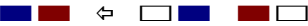
PRECISION REDUCTION (DATA PACKING) OPERATIONS: 32-BIT DATA		
PRECRQ.PH.W	Rd, Rs, Rt	$R_D = R_{S_L} \parallel R_{T_L}$ 
PRECRQ_RS.PH.W	Rd, Rs, Rt	$R_D = @[R_S^{\pm}]_L \parallel @[R_T^{\pm}]_L$ 
PRECR_SRA.PH.W ^{R2}	Rd, Rs, SHIFT5	$R_D = (R_D^{\pm} \gg \text{SHIFT}5)_R \parallel (R_S^{\pm} \gg \text{SHIFT}5)_R$
PRECR_SRA_R.PH.W ^{R2}	Rd, Rs, SHIFT5	$R_D = @[R_D^{\pm} \gg \text{SHIFT}5]_R \parallel @[R_S^{\pm} \gg \text{SHIFT}5]_R$

ACCUMULATOR EXTRACT OPERATIONS: 32-BIT DATA		
EXTR.W	Rd, Ac, SHIFT5	$R_D = (Ac \gg \text{SHIFT}5)_R$
EXTR_R.W	Rd, Ac, SHIFT5	$R_D = @[Ac \gg \text{SHIFT}5]_R$
EXTR_RS.W	Rd, Ac, SHIFT5	$R_D = @[Ac \gg \text{SHIFT}5]_R$
EXTRV.W	Rd, Ac, Rt	$R_D = (Ac \gg R_{T40})_R$
EXTRV_R.W	Rd, Ac, Rt	$R_D = @[Ac \gg R_{T40}]_R$
EXTRV_RS.W	Rd, Ac, Rt	$R_D = @[Ac \gg R_{T40}]_R$

BIT-FIELD EXTRACT OPERATIONS		
BPOSGE32	OFF18	IF POS ≥ 32, PC += OFF18 [±]
EXTP	Rd, Ac, SIZE5	$R_D = Ac_{\text{POS:POS-SIZE}5}$
EXTPDP	Rd, Ac, SIZE5	$R_D = Ac_{\text{POS:POS-SIZE}5}, \text{POS} -= (\text{SIZE}5 + 1)$
EXTPV	Rd, Ac, Rs	$R_D = Ac_{\text{POS:POS-RS}40}$
EXTPDPV	Rd, Ac, Rs	$R_D = Ac_{\text{POS:POS-RS}40}, \text{POS} -= (RS_{40} + 1)$
MTHLIP	Rs, Ac	$Ac_{HI} = Ac_{LO}, Ac_{LO} = Rs, \text{POS} += 32$

LOAD DATA OPERATIONS		
BITREV	Rd, Rs	$R_D = R_{S_{0:15}}$
LBUX	Rd, Rs(Rt)	$R_D = \text{MEM}8(R_S + R_T)^{\circ}$
LHX	Rd, Rs(Rt)	$R_D = \text{MEM}16(R_S + R_T)^{\pm}$
LWX	Rd, Rs(Rt)	$R_D = \text{MEM}32(R_S + R_T)$
MODSUB	Rd, Rs, Rt	$R_D = (R_S \neq 0) ? (R_S - R_{T7:0}) : R_{T23:8}$

ACCUMULATOR OPERATIONS		
MFHI	Rd, Ac	$R_D = Ac_{HI}$
MFLO	Rd, Ac	$R_D = Ac_{LO}$
MTHI	Rs, Ac	$Ac_{HI} = Rs$
MTLO	Rs, Ac	$Ac_{LO} = Rs$
SHILO	Ac, SHIFT6	$Ac = (\text{SHIFT}6^{\pm} \geq 0) ? (Ac \gg \text{SHIFT}6^{\pm}) : (Ac \ll -\text{SHIFT}6^{\pm})$
SHILOV	Ac, Rs	$Ac = (R_{S_{5:0}}^{\pm} \geq 0) ? (Ac \gg R_{S_{5:0}}^{\pm}) : (Ac \ll -R_{S_{5:0}}^{\pm})$

BIT-FIELD OPERATIONS		
APPEND ^{R2}	Rd, Rs, SHIFT5	$R_D = (R_D \ll \text{SHIFT}5) :: R_{S_{\text{SHIFT}5-1:0}}$
BALIGN ^{R2}	Rd, Rs, BPOS2	$R_D = (R_D \ll (8 \times \text{BPOS}2)) :: (R_S \gg (32 - 8 \times \text{BPOS}2))$
INSV	Rd, Rs	$R_{D_{\text{POS}+SIZE-1:\text{POS}}} = R_{S_{\text{SIZE}-1:0}}$
PACKRL.PH	Rd, Rs, Rt	$R_D = R_{S_R} \parallel R_{T_L}$ 
PREPEND ^{R2}	Rd, Rs, SHIFT5	$R_D = R_{S_{\text{SHIFT}5-1:0}} :: (R_D \gg \text{SHIFT}5)$