

Features

A complete system for coherent multiprocessing, including:

- 1 to 4 1004K multi-threaded “base” cores (up to 8 hardware threads)
- Coherence Management (CM) unit – the system “glue” for managing coherent operation between cores and I/O
- I/O Coherence Unit (IOCU) – hardware block for offloading I/O coherence from software implementation on CPUs
- Cluster Power Controller (CPC) – multi-core power management
- Global Interrupt Controller (GIC) – system and inter-processor interrupt controller
- Extended 256-bit interface to L2 cache controller, and 256-bit interface from L2 Cache controller to rest of system (available separately)
- EJTAG/PDtrace™ block for advanced debug/trace of complete coherent system

1004K Base Core

- 9-stage pipeline delivering more than 2.9 Coremark/MHz per core
- Based on 34K™ series cores, with cache coherency support added
- Supports single- or dual-threaded operation per core
- Uses Virtual Processing Elements (VPEs) for hardware multi-threading
- Integer (1004Kc™) and floating point (1004Kf™) versions
- Support for Revision 1 of MIPS32 DSP ASE
- Coherency port has duplicate data cache tags for background coherency checks
- Design-time configurability for inclusion and sizing of instruction and data TLBs, caches, scratchpad RAM and other options

Floating Point Unit (FPU)

- 1004Kf core has IEEE 754-compliant FPU, compliant to MIPS® 64-bit FPU architecture
- Supports single- and double-precision data types
- Separate in-order, dual-issue pipeline decoupled from integer pipeline

Coherency Management (CM) Unit

- Manages coherency using the MESI protocol
- Operates at same clock (1:1) as CPUs for maximum performance
- 256-bit extended interface for maximum throughput to (optional) L2 cache controller
- Supports performance enhancements via L1 cache-to-cache transfers, speculative reads to external memory, and globalized cache operations
- Global Configuration Registers (GCRs) for configuring/controlling CM scheme

Cluster Power Controller

- Provides highly scalable performance/power management via shutdown and bring up of one or more cores in the coherent processing system
- Works in conjunction with each core implemented in a separate power domain

I/O Coherence Unit (IOCU)

- Bridges non-coherent I/O peripheral transfer and makes transactions coherent
- Supports per-transaction attributes for snooping L1 caches, L1+L2 caches, or non-coherent transactions, plus I/O prioritization

Global Interrupt Controller (GIC)

- Supports system-level interrupts; inter-processor interrupts
- Routes interrupts to particular core or VPE
- Configurable # of system interrupts (up to 256)

Development Tools

- MIPS® Navigator ICS - IDE, software toolkit, MIPSsim™, EJTAG and PDtrace probes
- CodeSourcery - SG++ toolchains for MIPS

Uses multi-threading
to deliver maximum
performance from
each core