MIPS® cJTAG Adapter User's Manual

1 Introduction

MIPS provides an IEEE 1149.1-compatible JTAG debug and control port called EJTAG for its processor cores. Recently, an updated IEEE standard, 1149.7, has been published. One of the enhancements is a reduction in the number of external signals required from four to two. For some chip designs, pin count is critical, and the ability to provide debugging capabilities with only two pins could be crucial.

MIPS provides a cJTAG Adapter IP block that converts a 2-pin 1149.7 (also known as cJTAG) to the 4-pin 1149.1 debug interface present on MIPS cores. The IP resides outside the core and is treated as a separate IP block from the point of view of design verification and implementation.

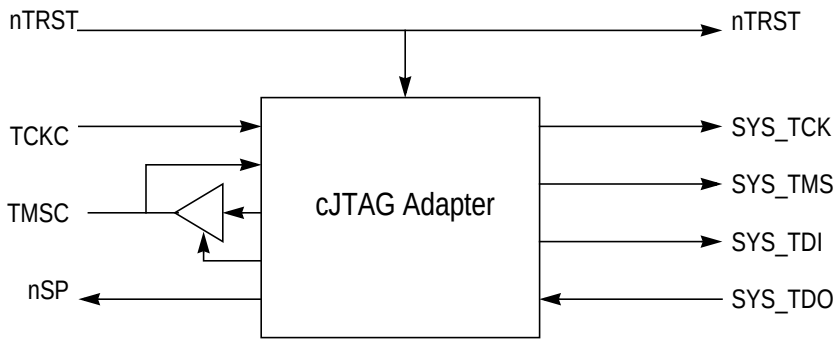
MIPS debug probes will be enhanced to support both cJTAG and legacy EJTAG. EJTAG and cJTAG use the same 14-pin connector called out in the MIPS EJTAG Specification, but when connected to cJTAG, the TDI and TDO signals are not used.

The IEEE1149.7 Specification is complex and much more flexible than is needed in this application. The IP implemented here is a subset of 1149.7.

2 Overview

The cJTAG Adapter provides a probe interface consisting of two signals—TCKC and TMSC—and a device interface consisting of four signals—SYS_TCK, SYS_TMS, SYS_TDI, and SYS_TDO. The TMSC signal is bidirectional, so the Adapter separates the signal into three ports—TMSC_IN, TMSC_OUT, and TMSC_EN—and requires the system designer to provide the appropriate attachment to a bidirectional device pin. TCKC is sourced from the probe (called DTS in the IEEE Specification). TMSC is bidirectional and carries control information to the Adapter and data in both directions.

Figure 1 cJTAG High Level Pins



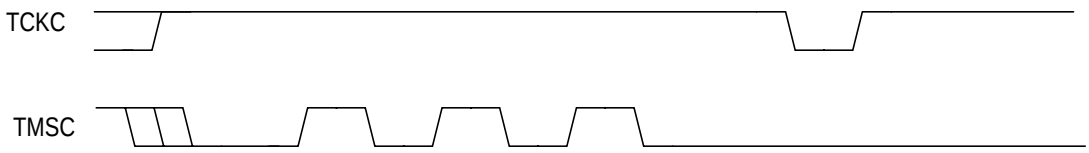
3 Protocols

3.1 Online/Offline

The Adapter can be either online or offline. When the Adapter is offline, activity on the TCKC and TMSC signals does not affect the 1149.1 port. When online, TCKC and TMSC indirectly drive the 1149.1 port to perform JTAG scans. There is a protocol to switch between the online and offline states.

When the Adapter is reset, it is in the offline state. A reset can be performed using the optional nTRST signal or through a sequential protocol on TCKC/TMSC. Switching online or offline and performing reset are accomplished using an Escape sequence described in the IEEE 1149.7 Specification. While TCKC is held high, TMSC is toggled a certain number of times. The Adapter keeps a count of the number of edges observed on TMSC and executes the corresponding command at the next TCKC rising edge.

Figure 2 cJTAG Online



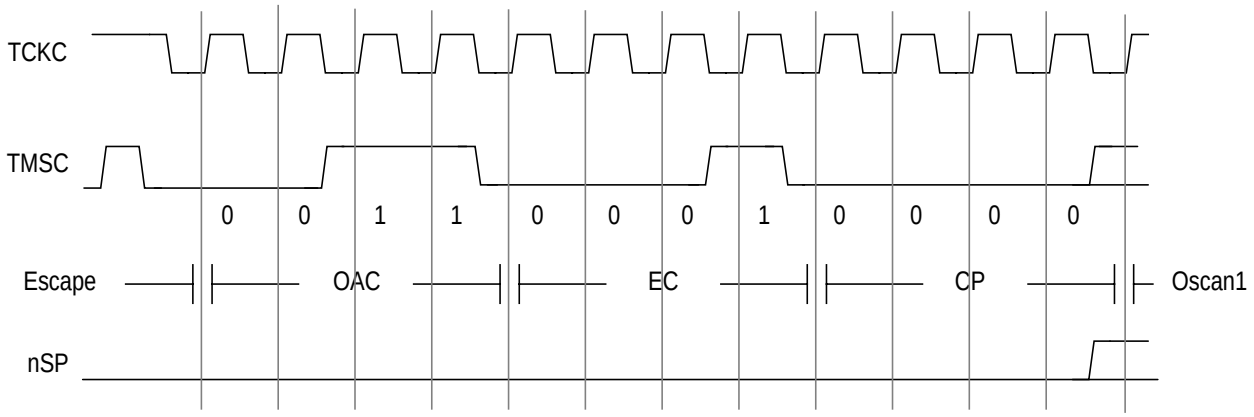
As described in the IEEE Specification, there may be a TMSC edge coincident with the last rising edge of TCKC before the Escape sequence begins, and that edge may or may not be detected by the Escape logic, depending on signal skew. A single pulse that would normally be two edges could therefore be counted as three edges. Escape detection logic takes this possibility into account. The Adapter interprets TMSC edges in an Escape as described in the following subsection.

3.2 Online Activation Code

Following the Online Escape sequence, the probe transmits an Online Activation Code (OAC), Extension Code (EC), and Check Packet (CP), for a total of 12 TCKC pulses. The Adapter observes the control data in these codes and activates only if the requested protocol variations are supported by the Adapter. In this implementation, only one form of activation code is supported; any other sequence of control bits will return the Adapter to the offline state.

Referring to the IEEE Standard, the OAC required is 1100, transmitted LSB first, which connotes TAP.7 star-2 scan topology. The EC must be 1000, indicating the short form and use of the Run-Test/Idle TAP state when switching online or offline. The CP is 0000. At the rising edge of TCKC in the last bit of the CP, the Adapter is activated. From that point forward, activity on TCKC/TMSC is interpreted as Oscan1 format, described in the IEEE Standard, until the Adapter is reset or otherwise taken offline.

Figure 3 cJTAG Online Activation Code

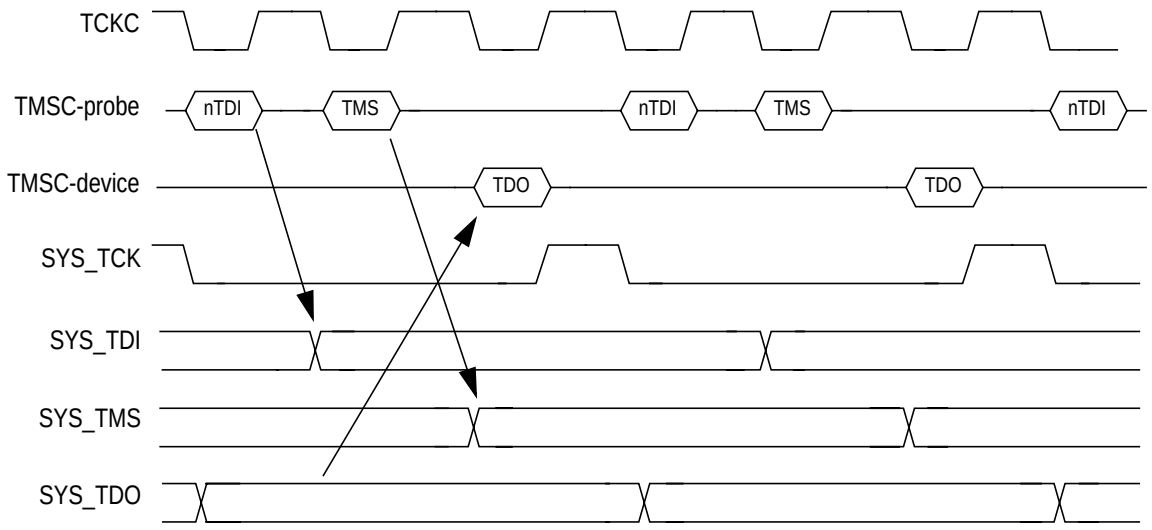


3.3 Oscan1

Once activated, the Adapter supports only the Oscan1 format. In Oscan1 format, the TMS, TDI, and TDO signals to the device are multiplexed onto the TMSC signal to the probe. Three TCKC pulses are required to perform one bit of JTAG scan. Per the IEEE Standard, the first bit of each 3-bit group (called a Scan Packet or SP) is the inverse of the TDI signal, denoted nTDI. This is followed by TMS and finally TDO. The probe drives TMSC during the first two bit periods, and the device drives TMSC during the last bit period.

To avoid a drive conflict in Advanced Protocol (Oscan1), TMSC is driven by its source only while TCKC is low, and relies on a system-level keeper circuit to maintain a valid logic level while TCKC is high.

Figure 4 cJTAG Online Activation Code



4 Chip Pin Requirements

The IEEE Specification requires all system designs to implement inputs with the characteristics shown in Table 1. To support this, the Adapter provides an output signal, nSP, that indicates the Standard Protocol is active.

Table 1 cJTAG Chip Pin Requirements

External Signal	Power Off	Power On, nSP=0	Power on, nSP=1
TCKC	Undefined	Pull-up	Pull-up
TMSC	Undefined	Pull-up	Keeper

Care should be taken to minimize the load on TCKC and TMSC, since many components may be controlled from a single driver. Because these are both edge-triggered signals, care must be taken in system implementations to avoid reflections and other signal degradation that could cause incorrect operation. In large designs with more than one load, pull-up and keeper circuitry may need to be implemented at the board-level rather than the chip-level.

5 RTL

The MIPS cJTAG Adapter IP block is located in a single RTL file at `$MIPS_PROJECT/proc/design/rtl/mips_cjtag.v`, as part of the MIPS softcore package. If the cJTAG interface is not needed, the cJTAG Adapter IP block can be totally ignored. If the cJTAG interface is needed, SoC integrators should instantiate and connect the cJTAG Adapter IP block in the design as described in the next section.

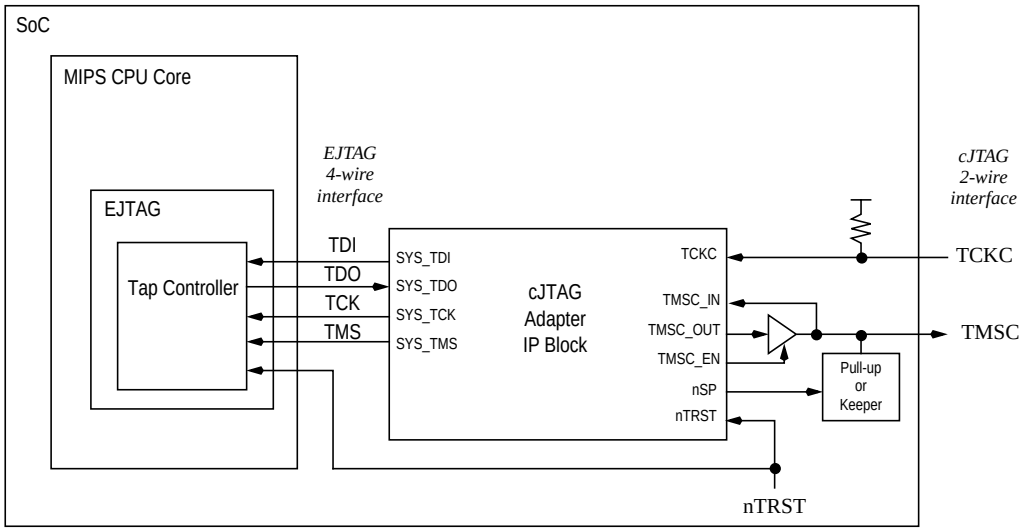
Note that the cJTAG interface is purely a hardware conversion function and is transparent to software—there are no configuration, control, or status registers associated with the cJTAG interface.

6 Integration

The cJTAG Adapter IP block is provided as a separate IP block outside the MIPS CPU Core. Figure 5 illustrates a typical design showing how the cJTAG Adapter is integrated in an SoC. It is preferable to synthesize both the MIPS CPU core and the cJTAG Adapter together to ease the timing constraints of the 4-wire EJTAG interface between the MIPS CPU Core and the cJTAG Adapter.

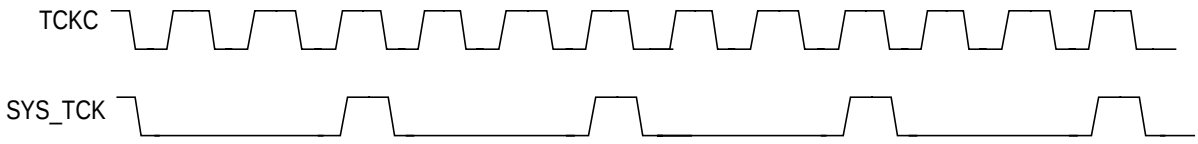
An nTRST signal can be provided in the same way for cJTAG and EJTAG interfaces, that is, it can be provided externally as an input pin to the SoC, or it can be generated internally by the SoC in order to reset the TAP circuitry using on-chip power-on reset logic.

Figure 5 cJTAG Integration



The clock of cJTAG (*TCKC*) interface and EJTAG (*SYS_TCK*) interface operate synchronously with a 3X speed ratio as shown in Figure 6. *SYS_TCK* is generated based on *TCKC* inside the cJTAG block by masking out 2 of the pulses every 3 cycles. It is important to constrain *TCKC* with a 3X frequency as the normal clock will run in the EJTAG block.

Figure 6 TCKC and SYS_TCK

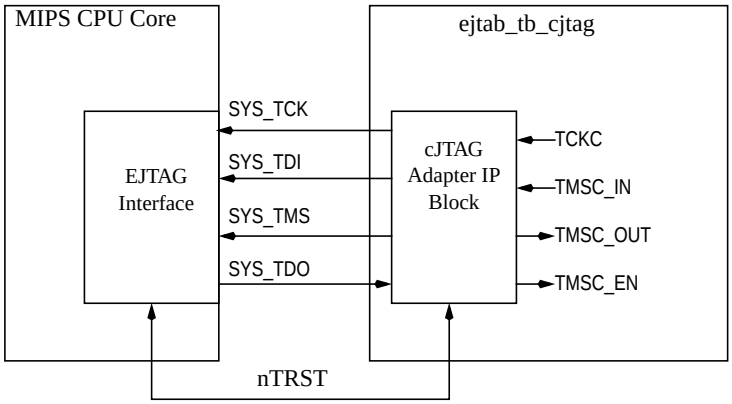


For the rest of the cJTAG signals *TMSC_**, they should be constrained in a similar way as input *TDI* and *TMS*, and output *TDO*, like in the 4-wire EJTAG interface when the cJTAG Adapter is not in used.

7 Testing

The cJTAG Adapter IP block is instantiated under the MIPS softcore testbench environment in a file named ‘`ejtag_tb_c_cjtag`’. The testbench performs as a 2-wire debugger, sending the Escape sequence, Online Active code, and Oscan1 to the Adapter. Figure 7 illustrate the cJTAG testbench environment.

Figure 7 cJTAG Test Environment



To see how the adapter works, TAP-related test cases such as '`tap_fastdata-ebm32k-cjtag-zws`' can be run under a normal softcore testbench environment. Without the '`-cjtag-`' mode string, the test cases will run with the normal EJTAG (IEEE1149.1) interface, bypassing the Adapter.

More testcases are also available to check the adapter:

```
tap_procacc1-ebm32k-cjtag-zws-prgint
tap_procacc3-ebm32k-cjtag-zws-prgint
tap_procacc4-ebm32k-cjtag-zws-prgint
tap_implreg-ebm32k-cjtag-zws-prgint
cJTAG_active-ebm32k-cjtag-zws-prgint
tap_fastdata-ebm32k-cjtag-zws-prgint
```

8 References

1. MIPS® EJTAG Specification
   MIPS document: MD00047

2. IEEE Std 1149.7™-2009, IEEE Computer Society, New York NY, 2010

9 Revision History

Change bars (vertical lines) in the margins of this document indicate significant changes in the document since its last release. Change bars are removed for changes that are more than one revision old.

Date	Revision	Description
June 16, 2011	01.00	Initial release

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