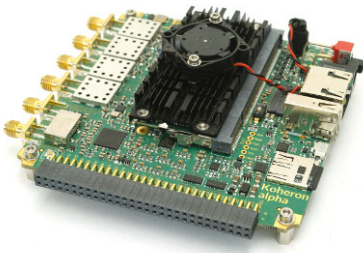


# ALPHA250 - 250 MSPS acquisition board



The ALPHA250 is a programmable board built around a Zynq 7020 SoC. It features a 100 MHz RF front end with dual 14-bit ADC 250 MSPS and dual 16-bit DAC 250 MSPS. Analog input to output latency is less than 90 ns. The RF ADC and DAC are clocked by a dual PLL, ultra-low jitter clock generator. It includes a 4 channel 24-bit ADC and 4 channel 16-bit DAC. The board comes with a comprehensive, open source, FPGA / Linux reference design.

## Includes

- Koheron ALPHA250 board
- 12 V 1.5 A power supply
- Micro-SD card with pre-installed OS

## Specifications

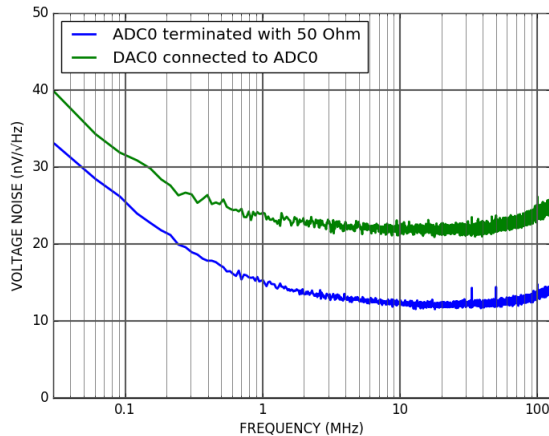
### ALPHA250

<b>Programmable logic, processor and memory</b>	
System On Chip	Zynq 7020 XC7Z020-2CLG400I
Memory	512 MB of DDR3L SDRAM
Processor	ARM dual-core CPU
<b>100 MHz low-noise RF front-ends</b>	
RF ADC	2 channels, 14-bit, 250 Msps, DC coupled
RF DAC	2 channels, 16-bit, 250 Msps, DC coupled
Input to output latency	90 ns
Input / Output	1 V <sub>pp</sub> , 50 Ω
<b>Ultra-low jitter clock generation for RF ADC, DAC and FPGA</b>	
Clock generator	Dual loop PLL, 100-fs RMS jitter (12 kHz to 20 MHz)
On-board VCXO	160 dBc / Hz @ 10 kHz
Reference clock inputs	FPGA, external clock or internal crystal oscillator
On-board TCXO	10 MHz, 280 ppb
<b>Precision analog monitoring and control</b>	
Precision ADC	4 channels, 24-bit
Precision DAC	4 channels, 16-bit
Voltage reference	2.5 V, low-drift (3 ppm/°C)
Temperature sensor	±0.2 °C accuracy
<b>Other</b>	
Connectivity	10/100/1000 Ethernet, USB 2.0, USB-UART
General purpose I/O	16 FPGA I/Os (3V3), 8 user LEDs
Dimensions	10 cm x 10 cm
<b>Software</b>	
OS	Ubuntu 16.04
Reference designs	FFT Analyzer, ADC / DAC with BRAMs, ADC / DAC with DMA, Phase noise analyzer, Loopback

## Characterization

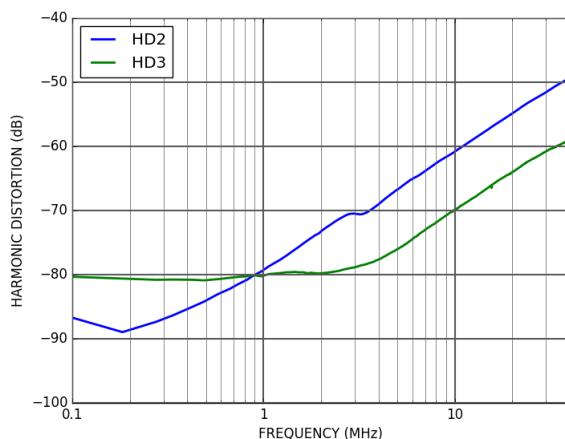
### Noise floor

The RF ADC and DAC noise floors were characterized with this script [available on GitHub](#). The input referred voltage noise density of the ADC is about 13 nV/ $\sqrt{\text{Hz}}$ . DAC voltage noise density is about 23 nV/ $\sqrt{\text{Hz}}$  (19 nV/ $\sqrt{\text{Hz}}$  after subtraction of the ADC noise floor).



### Distortion

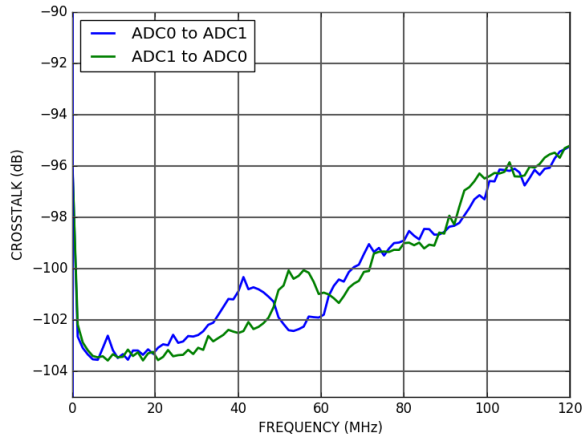
A 1 Vpp sine wave between 100 kHz and 40 MHz was sent by DAC0 and measured by ADC0 ([see script](#)). The figure below shows the amplitude of the second and third harmonic, relative to the fundamental frequency:



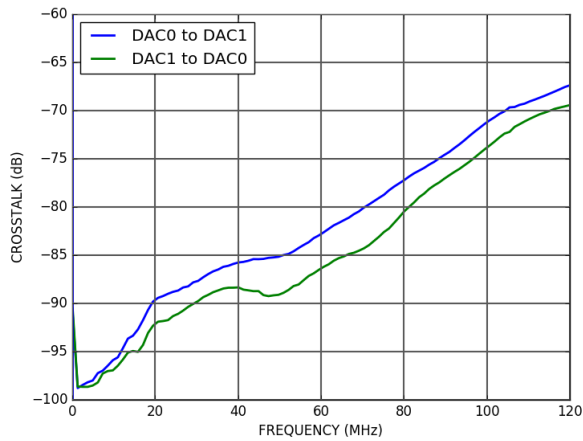
Distortion performance is limited by the DAC. ADC distortion (HD2 and HD3) stays under -80 dB up to 40 MHz.

### Crosstalk

The crosstalk between the 2 ADC channels was characterized with the following [script](#). Crosstalk is under -95 dB up to 120 MHz.



Crosstalk between the two DAC channels is shown below:



## Phase Noise

The phase noise of a 10 MHz OXCO reference clock (from Textronix MCA 3027) against the internal TCXO was measured with the [Phase Noise Analyzer](#) reference design:

