Supporting Information for

Quantitative, Dynamic TaO$_x$ memristor/Resistive Random Access Memory Model

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In the proposed model, the three PDEs in Eqs (2), (5), and (6) were self consistently solved through a numerical solver (COMSOL) to calculate $n_D$, $\Psi$, and $T$. Figure S1 shows the structure used in the model. The width ($w$) and depth ($d$) of the structure is 40 nm and 20 nm, respectively. The thicknesses of the Pd bottom electrode (BE), $V_O$ reservoir (TaO$_x$) layer, switching (Ta$_2$O$_5$) layer, and the Pd top electrode (TE) layer are 35 nm, 30 nm, 5 nm, and 50 nm, respectively. The $V_O$ density of $5 \times 10^{21}$ cm$^{-3}$ is chosen as a criteria for metallic CF formation, and the maximum $V_O$ density is $\sim 1 \times 10^{22}$ cm$^{-3}$. A uniform concentration of $n_D = 1 \times 10^{22}$ cm$^{-3}$ is assumed in the conductive TaO$_x$ layer as an initial state. The current modulation layer (CML) height ($h$) is 10 nm, which is directly connected to TE.

The following assumptions are used as boundary conditions: the temperature at BE, TE and CML surfaces are 300 K, BE is always grounded during simulation, while voltage is applied to the top of CML. The definition of the parameters and constant values used in the model are summarized in Table S1 and Figure S2a. The electrical conductivity is given by the Arrhenius equation where the pre-exponential factor $\sigma_0$ is assumed to linearly increase from 1 S/m to $10^5$ S/m with increasing $n_D$. The electron conduction activation energy $E_{AC}$ used in the model is 0.2 eV for the initial state where $n_D$ is $1 \times 10^{16}$ cm$^{-3}$, and linearly decreases to 0.1 eV with increasing $n_D$ up to $1 \times 10^{20}$ cm$^{-3}$, 0 eV with $n_D$ up to $5 \times 10^{21}$ cm$^{-3}$, and -0.006 eV with $n_D$ up to $1 \times 10^{22}$ cm$^{-3}$. The pre-factor of thermal conductivity $k_{th0}$ linearly increases with increasing $n_D$ (Figure S2b).

To introduce the compliance current ($I_{CC}$) during Forming and Set, the conductance of the CML is defined by Eqs (S1a) – (S1c). Here, $V_1$ is voltage applied to the CML top surface and $V_2$ represents the actual voltage applied on the memristor TE, as shown in Figure S1. If the electrical field applied to CML is smaller than $E_{\text{MAX}}$, the conductance of CML will be $I_{cc,\text{Sigma}}$, $10^5$ S/m,
while when the electric field becomes larger than $E_{\text{MAX}}$ the conductance of the CML is determined by Eq. S1a. During Reset, $\sigma_{\text{CML}}$ is always $I_{\text{cc, Sigma}}$, $10^5$ S/m.

$$\sigma_{\text{CML}} = \frac{I_{\text{cc}} \cdot h}{|V_1 - V_2| \cdot w \cdot d}, \quad \text{if } E_{\text{CML}} \geq E_{\text{max}} \quad (S1a)$$

$$\sigma_{\text{CML}} = I_{\text{cc, Sigma}}, \quad \text{if } E_{\text{CML}} < E_{\text{max}} \quad (S1b)$$

$$E_{\text{max}} = \frac{I_{\text{cc}}}{I_{\text{cc, Sigma}} \cdot w \cdot d} \quad (S1c)$$

where $h = 10$ nm, $w = 40$ nm, $d = 20$ nm, $I_{\text{CC}} = 500$ $\mu$A.

To model the transistor $I$-$V$, conductance of CML is defined in Eqs (S2a) – (S2d) $^{57}$.

$$\sigma_{\text{CML}} = \left( \frac{W}{L} C_{\text{ox}} \mu \left( V_{gs} - V_t - \frac{m(V_1 - V_2)}{2} \right) \right) \frac{h}{1 + \frac{V_1 - V_2}{E_{\text{sat}} L}} \cdot \frac{d \cdot w \cdot (V_1 - V_2)}{d \cdot w \cdot (V_1 - V_2)}$$

$$\sigma_{\text{CML}} = \left( \frac{W}{L} C_{\text{ox}} \mu \left( V_{gs} - V_t - \frac{mV_{\text{dsat}}}{2} \right) \right) \frac{h}{1 + \frac{V_1 - V_2}{E_{\text{sat}} L}} \cdot \frac{d \cdot w \cdot (V_1 - V_2)}{d \cdot w \cdot (V_1 - V_2)} \quad (S2a)$$

$$\sigma_{\text{CML}} = \left( \frac{W}{L} C_{\text{ox}} \mu \left( V_{gs} - V_t - \frac{mV_{\text{dsat}}}{2} \right) \right) \frac{h}{1 + \frac{V_1 - V_2}{E_{\text{sat}} L}} \cdot \frac{d \cdot w \cdot (V_1 - V_2)}{d \cdot w \cdot (V_1 - V_2)} \quad (S2b)$$

$$V_{\text{dsat}} = \frac{2(V_{gs} - V_t) / m}{1 + \sqrt{1 + 2(V_{gs} - V_t) / m E_{\text{sat}} L}} \quad (S2c)$$

$$E_{\text{sat}} = \frac{2v_{\text{sat}}}{\mu} \quad (S2d)$$

where $L = 130$ nm, $W = 450$ nm, $m = 1.3$, $T_{\text{ox}} = 4$ nm, $\mu = 50$ cm$^2$/(V·s), $V_T = 0.3$ V, $v_{\text{sat}} = 8 \times 10^6$ cm/s, $a = 8 \times 10^{-6}$, $h = 10$ nm, $w = 40$ nm, and $d = 20$nm.

Figure S3 shows the $I$-$V$ behavior of the CML layer. The CML layer can effective model the effects of $I_{\text{CC}}$ and the transistor $I$-$V$, and match well with experimental results.
Figure S1. Device geometry used in the simulation. A uniform doping concentration of $n_D = 1 \times 10^{22}$ cm$^{-3}$ was assumed within the conducting TaO$_x$ layer ($V_O$ reservoir) at the initial state. $w = 40$ nm, $h = 10$ nm, $d = 20$ nm were used in the simulation. $V_1$ is the voltage applied to the current modulation layer top surface and $V_2$ represents the actual voltage applied to the memristor TE.
Table S1. Material parameters and constants used in the proposed model.
Figure S2. Parameters used in the proposed model. (a) The electrical conductivity pre-factor $\sigma_0$ and the electron conduction activation energy $E_{AC}$ as function of $n_D$. (b) The thermal conductivity pre-factor $k_{th0}$ as function of $n_D$. 
Figure S3. Current modulation layer $I$-$V$ behavior, without memristor devices. (a) Simulated DC $I$-$V$ with $I_{CC}$ of 500 μA. (b) Simulated and measured transistor DC $I$-$V$ curves with varying $V_G$ from 1 V to 4 V. The simulation results very well matched with experimental results.
Figure S4. Evolution of $V_O$ concentration ($n_D$) and temperature ($T$) during DC Forming. (a) DC $I$-$V$ characteristics during Forming. (b) 1D profile of temperature along the $z$ direction during Forming with different voltages. 2-D maps of (c) $n_D$ and (d) $T$ during Forming with different voltages.
Figure S5. Simulated RS behavior with different $I_{CCs}$. (a-c): 2-D maps of $n_D$ for (a) Forming, (b) Reset, and (c) Set processes with 300 µA of $I_{CC}$, along with the simulated DC $I$-$V$ characteristics (d). (e-g) 2-D maps of $n_D$ for (e) Forming, (f) Reset, and (g) Set process with 800 µA of $I_{CC}$, along with the simulated DC $I$-$V$ characteristics (h).
Figure S6. 2-D maps of $n_D$ profile after Set, for different Set $I_{CCs}$. The devices first goes through (a) Forming with 300 μA $I_{CC}$ and 1st Reset, or (b) Forming with 500 μA $I_{CC}$ and 1st Reset, respectively. Different $V_O$ configurations are observed during Set, for devices formed at these different Forming conditions, even if the same Set $I_{CCs}$ are used.
**Figure S7.** Simulated LTP behaviors with incremental $I_{CC}$, for different Forming conditions. Forming with lower $I_{CC}$ provides a larger dynamic range, but a steeper slope which may make it more difficult to fine-tune the conductance.
**Figure S8.** Set and Reset pulse simulation. (a) Current and (b) temperature evolutions at the location ‘A’ at different Set voltages. (c) Set speed vs. Set voltage. (d) Current and (e) temperature evolutions at the location ‘B’ at different Reset voltages.
**Figure S9.** Forming and switching characteristics vs. Ta$_2$O$_5$ film thickness. (a) I-V characteristics showing the Forming, and subsequent Reset and Set processes. (b) 2-D maps of $n_D$ profile after Forming, first Reset, and subsequent Set, for devices with different Ta$_2$O$_5$ film thicknesses.

**Figure S10.** Forming and switching characteristics vs. device area (20nm, 40nm, and 100nm).
Figure S11. Forming/Reset/Set switching characteristics as a function of ambient temperature, showing the (a) Forming, (b) first Reset, and (c) subsequent Set processes at different ambient temperatures.
Figure S12. Schematic of the 1T1R structure. (a) Cross-sectional view of the 1T1R structure with Pd/Ta$_2$O$_5$/TaO$_x$/Pd bilayer memristor device. (b) Top view. The BE of the memristor is connected to the Drain of the transistor to provide negative Forming and Set voltages to the memristor device.
Figure S13. Evolution of internal electric field distribution, at different stages of the Forming process.
SUPPORTING REFERENCES


