Supporting Information

Three-Dimensional Nanoscale Flexible Memristor Networks with Ultralow Power for Information Transmission and Processing Application

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Figure S1. The surface morphology of HfAlO$_x$ on different substrates were measured using AFM in the tapping mode, where HfAlO$_x$ film was prepared by low-temperature atomic layer deposition (ALD) process at 130°C. The root-mean-square average roughness (Rq) of HfAlO$_x$ on (a) silicon and (b) PET substrate is 2.01nm and 3.48nm, respectively.
S2. Spike-voltage dependent plasticity (SVDP) of artificial synapse under negative pulses.

**Figure S2.** The depression characteristics of memristors under 50 negative pre-synaptic pulses with different amplitudes of -0.2V, -0.4V, -0.6V, -0.8V and -0.9V. The initial PSC before simulation is ~20uA. The PSC after 50<sup>th</sup> synaptic spikes under different pulses was 16.3uA, 15.3uA, 14.9uA, 13.6uA and 13.0uA, respectively. During depression process, the degree of inhibition would be enhanced with the increase of voltage amplitude, indicating the SVDP characteristic of artificial synapse was realized under negative pulses.
S3. Mechanism of synaptic plasticity in memristors.

Figure S3. Schematic illustrations of long-term potentiation/depression (LTP/LTD) behaviors in artificial synapse. The LTP/LTD behaviors were measured via applying pulses to the top electrode of memristor in 1st layer and recorded the output of bottom electrode of memristor in 1st layer. (a-c) With consecutive positive voltage applied to top electrode, the oxygen vacancy accumulated in bottom electrode and formed conductive path between top electrode and bottom electrode, resulting to the potentiation of conductance. (d-f) The rupture of conductive path would occur when negative voltage was applied to top electrode, corresponding to the depression process of synaptic device.
S4. Phenomenon of abrupt conductance modulation.

**Figure S4.** The abrupt change behavior of conductance modulation in our device. The schematic illustration of electrical spikes for simulating LTP/LTD with pulse width of (a) 1ms and (b) 100us. (c) LTP/LTD inspired by pre-pulses (pulse amplitude=1.1V/-1.1V, pulse width= 1ms, pulse number=150) with abrupt conductance modulation. (d) LTP/LTD inspired by pulses (pulse amplitude=1.1V/-1.1V, pulse width= 100us, pulse number=150). It should be noticed that the conductance changed abruptly when 151\textsuperscript{th} pulse applied to the device, which is not suitable for neuromorphic computing\textsuperscript{[1-3]}. The results show that the pulse width of 1ms and 100us are too wider for continuous conductance modulation with the pulse amplitude of 1.1V/-1.1V.
S5. Ultra-multistate conductance modulation with different level spikes.

Figure S5. The ultra-multistate conductance modulation could be realized by adjusting amplitudes of pre-spike. (a) The schematic diagram of pulse waveform used for simulating ultra-multistate conductance modulation. The LTP behavior was emulated by consecutive positive pulses (pulse amplitude= 1.4V, pulse width= 10us, pulse number= 150). The LTD characteristic was simulated by two level negative pulses (Level 1: pulse amplitude= -0.5V, Level 2: pulse amplitude= -1V, pulse width= 10us, pulse number= 150). (b) LTP and LTD with ultra-multistate emulated by 450 consecutive pulses. The LTD behavior was simulated with two level pulses, inducing 300 conductance states in depression process.
S6. LTP/LTD of three-layer memristors under flat and bending state.

**Figure S6.** The synaptic plasticity and flexibility of 3D crossbar memristors. A series of positive (pulse amplitude=1V, pulse width=10us, pulse duration=1ms) and negative (pulse amplitude=-1V, pulse width=10us, pulse duration=1ms) pre-synaptic spikes were applied to top electrode of each layer, the conductance of memristors was modulated gradually, simulating the LTP/LTD behaviors in (a) 1st layer, (b) 2nd layer and (c) 3rd layer artificial synapses. There are 50 conductance states in LTP and 50 conductance states in LTD, respectively. To verify the mechanical flexibility of wearable 3D artificial neural architecture, the three-layer devices were measured under bending radius of 5mm. LTP and LTD were successfully emulated in (d) 1st layer, (e) 2nd layer and (f) 3rd layer bending artificial synaptic devices, indicating the potential of device used in wearable neuromorphic computing system.
S7. EPSC response time of device fabricated at different temperatures.

Figure S7. (a) The response of device fabricated at 200°C when applying pulse (5V/50ns). (b) The response of device fabricated at 200°C when applying pulse (5V/1us). (c) The response of device fabricated at 300°C when applying pulse (5V/50ns). (d) The response of device fabricated at 300°C when applying pulse (5V/10us).
S8. PPF index of 3D neural network.

Figure S8. PPF index of three-layer artificial synaptic network, including (a) Neuron 1, (b) Neuron 2 and (c) Neuron 3, respectively. The PPF index was fitted via a double exponential decay function used in biology.

![Figure S9.](image)

**Figure S9.** MNIST digital recognition with hidden layers consisting of different number of neurons. The recognition rate could achieve (a) 19%, (b) 81.6%, (c) 83.6%, (d) 88.8% and (e) 89% with 8, 16, 32, 64 and 128 hidden neurons, respectively. Comprehensively considering recognition rate, simplification and training speed, artificial neural network with 64 hidden neurons was selected for pattern recognition simulation.
**S10. Output signals of digits during training process.**

Figure S10. The output signals of “1-9” increased with training epoch. (a) The digit “1”, (b) digit “2”, (c) digit “3”, (d) digit “4”, (e) digit “5”, (f) digit “6”, (g) digit “7”, (h) digit “8” and (i) digit “9” could be recognized from digits of “0-9” due to the largest output signal after 1000 training epochs. The output of target digit would increase while other would decreased to near zero. The change of output signals of “0-9” exhibited the training effect of artificial neural network during 1000 epoch.

**Reference**

