Supplementary Information

for

Nanoscopic electrolyte-gated vertical organic transistors with low operation voltage and five orders of magnitude switching range for neuromorphic systems

Christian Eckel\textsuperscript{1,2,\#}, Jakob Lenz\textsuperscript{1,\#}, Armantas Melianas\textsuperscript{3}, Alberto Salleo\textsuperscript{3} and R. Thomas Weitz\textsuperscript{1,2,*}

\textsuperscript{1} AG Physics of Nanosystems, Faculty of Physics, Ludwig-Maximilians-University, 80539 Munich, Germany
\textsuperscript{2} 1\textsuperscript{st} Institute of Physics, Faculty of Physics, Georg-August-University, 37073 Göttingen, Germany
\textsuperscript{3} Department of Materials Science and Engineering, Stanford University, 94305 Stanford, California, USA

* Thomas.weitz@uni-goettingen.de

\#these authors contributed equally to this work
Materials and Methods

**EGOT fabrication:**

P-type silicon substrates with 300 nm SiO$_2$ layer are cleaned with isopropanol and acetone in an ultrasonic bath. The bottom contacts are patterned with photolithography as described below in the photolithography section. The width of the bottom contacts defines the channel width $w_C$ (see Fig. 1a in the main manuscript and Fig. S1). 1 nm chromium (Cr), 30 nm Gold (Au) and 1 nm titanium (Ti) are deposited in an UHV-evaporation chamber (Bestec, $p = 10^{-6}$ – $10^{-7}$ mbar), whereby Cr and Ti are used as adhesion layers. After lift-off in acetone the top contacts are patterned in the same manner. The thickness of the sputtered (Ardenne LS320) SiO$_2$ spacer defines the channel length $L_C$ ($P = 50$ W, argon pressure $p = 2 \times 10^{-2}$ mbar, see Figure 1a in the main manuscript). The top contacts with 1 nm Ti and 90 nm Au are done again via evaporation. In the next step, SiO$_2$ between the top and bottom contacts is etched for 80 s with a 1 % HF-solution resulting in an under-etched channel distance $d_C$ of around 80 nm (see Figure 1a in the main manuscript). The under etched region is filled with our PDPP OSC via spin-coating. The PDPP is dissolved in MDCB with a ratio of 15 mg/ml and is stirred overnight at 80 °C. Settings for the spin-coating: 40 s at 1000/min and a ramp of 1000 followed by a softbake for 2 min at 80 °C. The OSC is directional etched away with an RIE machine (Oxford PlasmaLab 100 ICP65) with an oxygen plasma (20 sccm, 20 mbar, 50 W), until the remaining OSC is solely under the top contact. A PEDOT:PSS droplet as gate electrode is placed next to the channel with a syringe and annealed for 10 min at 80 °C. Finally the EMIM:TFSI electrolyte is deposited over the channel with a syringe, building a connection to the PEDOT:PSS. An overnight bake in a vacuum oven at 10 mbar and 50 °C reduces moisture residues. An ozone clean atmosphere is ensured during all processing steps. The device dimensions for the used EGOTs are listed in Table S1. Top view microscope pictures of the devices can be found in Fig. S1-S3.

**Photolithography:**

As a photoresist we used AZ701 MIR combined with the adhesion coating Ti-Prime. For deposition, spin-coating is used with following settings. For Ti-Prime 10 s, 500 /min, 200 ramp followed by 30 s, 5000 /min, 1000 ramp with a 120 s, 90 °C softbake. The AZ701 MIR is spin-coated with 3 s, 800 /min 800 ramp followed by 30 s 6000 /min 4000 ramp with a 60 s, 90 °C softbake. A Maskaligner (KarlSuss MJB3) with a He-lamp as the source imprints the structure through a Cr mask with an exposure time of 90s. The development of the structure is done by immersing the sample for 30 s into AZ726 MIF followed by a DI-Water bath. The lift-off procedure after metal and SiO$_2$ deposition uses 3 x acetone and 1 x isopropanol in an ultrasonic bath with low power, each step taking 4 – 5 min.
Electrical measurement:

The electrical characterization measurements (transfer and output curve) are performed via two source-meter units (Keithley 2450). Except for Fig. S4, all synaptic measurements were performed in a vacuum chamber at pressures below $10^{-4}$ mbar. Source, drain and gate electrodes are contacted with Au bonding wires. For pulse generation, Keysight 3350B units were used. The currents are translated into voltages with transimpedance amplifiers DLPCA-200 and monitored with an RTB2004 oscilloscope. For synchronisation of the units and measurement evaluation, a customized software is used.

<table>
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<tr>
<th>Nr.</th>
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<th>Channel dimension</th>
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<td>Fig. 2a, S7</td>
<td>$L_C$ 35nm, $w_C = 12\mu m$, $d_C = 80$nm</td>
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<td>Fig. 2b-d</td>
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<td>Fig. 2e, Fig. 3c, Fig. 4d, Fig. S8, Fig. S9, Fig. 11, Fig. S13, Fig. S14, Fig. S15</td>
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<td>Fig. 4d, Fig. S15</td>
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<td>7</td>
<td>Fig. S4</td>
<td>$L_C$ 35nm, $w_C = 50\mu m$, $d_C = 80$nm</td>
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Table S1: EGOTs used in the figures of this article and their channel dimension.
1. Device pictures

**Supplementary Figure S1**: EGOT top view after RIE etching step.  
a) Optical microscope picture of top and bottom contact.  
b) Polarised microscope picture of the channel. OSC remains can be seen only in the underetched region below the top gold contact.

**Supplementary Figure S2**: SEM Picture. Original SEM Picture of Fig. 1b main manuscript. Side view of channel after RIE etching.
**Supplementary Figure S3: Top view of gated transistor.** In the bottom right is the PEDOT:PSS gate. The electrolyte droplet covers the channel of the transistor and connects it to the gate.
2. Electrical characteristic

Supplementary Figure S4: Exemplary electrical measurement of an EGOT: Measurements are taken in ambient atmosphere.

a) Transfer characteristics with sweep velocity 0.01V/s  
b) Output characteristics.
3. Switching Circuit

![Switching Circuit Diagram](image)

**Supplementary Figure S5: Switching circuit for the EGOT during a write and read-operation.** Switches S1-S4 are controlled by signals from the read-select (RS) and write-select (WS) inputs. a) During a write-pulse (WP), S3+4 are closed and the voltage is applied at the gate whereas the drain is floating. The gate-source-current $I_{GS}$ flows over the blue path. b) During a read-pulse (RP), S1+2 are closed and the voltage is applied at the drain whereas the gate is floating. The drain-source-current $I_{DS}$ flows over the green path.

The measurements for the conductance switching are performed using the electrical circuit of **Supplementary Fig. S5** (adapted from [1]). The main idea of the circuit is the decoupling of conductance change operation (write, Fig. S5a) and measuring the channel conductance (read, Fig S5b). For that purpose, four commercial transistors S1-S4 are placed around the EGOT. A write operation applies a write pulse (WP) at the gate while at the same time a synchronized signal at WS closes the switches S3 and S4. Hence, ions can penetrate into the channel and update the conductivity. The amount of penetrating ions is monitored by the gate-source-current $I_{GS}$. During a write-operation, the switches S1 and S2 are open to prevent any undesired currents. To extract the conductivity state, a read-pulse (RP) is applied at the drain of the EGOT together with a synchronized pulse at the RS to close the switches S1 and S2. With the measured drain-source-current $I_{DS}$ it is possible to calculate the conductivity with Ohm’s law and the drain voltage. Switches S3 and S4 are open, thereby hindering the discharging of the ions from the channel back into the electrolyte. The conductance state stays stable. In phases where no read or write pulse is applied, the EGOT is in a floating state due to the open switches S1-S4. Up/Down switching measurements (see Figure 2 in main manuscript) require three voltage levels at the gate: An Up/Down writing voltage and an Off-state voltage. During Off phases, the down writing voltage $V_{Down}$ is applied at WP. Due to the open switch S3 and the corresponding voltage drop over it 0 V effective bias is present at the gate. The pulses are generated by two Keysight 3350B wavegenerators. For monitoring the currents, an RTB2004 oscilloscope is used combined with a transimpedance amplifier DLPCA-200. For the switches we used an IC-EPP394 with 1 MΩ Off-resistance. One can assume that the 1 MΩ resistance, which is also present if no external voltage is applied, sufficiently prevents the discharging process.
4. Prolonged retention time

Supplementary Figure S6: Prolonged retention time. a) Circuit scheme for measuring EGOT with and without a switch at the gate. b) Measurement of drain current over time with (blue) and without (green) a gate switch. After applying 80 consecutive gate pulses (grey area) with 1 s duration, -0.8 V and 1 s pause the drain current is monitored for around 900 s with -0.1 V bias at the drain.

Increasing the stability of conductive states in memory devices is desired for most use cases. In section 4, the switching circuit for our measurements are described. To prove the prolonged retention times by using switches (i.e. to prevent discharging), a measurement with constantly monitored drain current over time is performed in Figure S6. In Figure S6a, the circuit schemes of the measurement are shown without and with a switch at the gate. The Off-resistance of the gate is 1 MΩ even without any external voltages. After applying 80 consecutive pulses, the drain current starts to decrease (see Figure S6b). The increased retention time with the switch (blue) compared to the one without (green) is clearly visible and assists our approach to minimize ion diffusion out of the channel. We believe that even higher resistance than the 1MΩ switch at the gate could increase the stability of the conductance. For instance, combining our devices at the gate similar to the work of Fuller et al. [2] with a conductive bridge memory (CBM), which exhibits an Off-Resistance of $10^{13}$ Ω [3], which is 7 orders of magnitude higher than the used ones, should significantly increase the retention time.

The necessity of stable conductance depends strongly on the use case. For instance, in DNNs where the synaptic weight values can be stored externally the retention times are sufficient in the multiple second regime compared to long time memory storage with multiple days or longer [4]. Newer network types as spiking neural networks are based on the conductance decay over time mimicking...
the synapses in human brains [5]. In section 9 and Figure 3 in the main article synaptic plasticity measurements of the EGOT are presented.
5. Deep Neural Network

Supplementary Figure S7: Artificial neural network. a) A three layer feedforward network architecture. Each neuron, marked as circles, is connected with all neurons from the previous and the following layer with different connection strengths $v_{ih}$ or $w_{ho}$. Information is traveling from the left to the right side. By applying a learning algorithm like the backpropagation algorithm, the network can be trained to optimize the output results. b) A crossbar array to realize a hardware based neural network. It shows the connection between the input and the hidden layer of a). The connection strengths are realized by memristors which have a tuneable conductance. Therefore, the current responses $I_{1/2}$ depend on the input voltages $V_{1/3}$ and the conductances $v_{ih}$. The connection $v_{11}$ and the corresponding memristor in the array are both marked in red.

Multiple architecture types for artificial neural networks (ANN) have been developed. One network commonly used is the deep neural network (DNN), which is based on a feedforward-inference architecture in combination with a backpropagation algorithm [6, 7]. Fig. S7a shows an example of a neural network. It consists of an input layer with three input neurons (yellow), two neurons in the hidden layer (blue) and three output neurons (green). Every neuron is connected with all neurons of the previous and the following layer. No interconnection within one layer is allowed. Information only passes from the left to the right and is encoded in the activation of the single neurons. The connection weight, similar to the synaptic strength, is given by $v_{ih}$ and $w_{ho}$. The number of layers and the amount of neurons in one layer are free to choose. Classical computers are build with a von Neumann architecture which entails processing problems in high data transfer tasks such as ANN [8]. To overcome this problem for computation in software-based networks, also referred to von Neumann bottleneck, a hardware realization with memristive devices can be used. It allows a highly parallel computing with the use of vector-matrix multiplication [4]. For that purpose, the devices are ordered in a crossbar array as shown in Fig. S7b. The activation of a neuron in such an array is represented by different voltage inputs, whereas the conductance of the memristive device emulates the corresponding synaptic weight. The sum of the currents over the memristive devices for each output path are translated into a voltage and serves as the input for the next layer.
6. High range switching Log-Log Plot

Supplementary Figure S8: High switching measurement. The plot shows the same data as in Fig. 2a of the main manuscript in a Log-Log diagram. Due to vertical resolution limitations of the used oscilloscope, the measurement is split into a high resolution (green) and low resolution (blue) part. Combining the two measurement runs results in a total switching range over 5 orders of magnitude. Settings: \( t_{\text{write}} = 10 \, \mu s \), \( V_{\text{write}} = -0.9 \, V \), \( t_{\text{read}} = 100 \, \text{ms} \), \( V_{\text{read}} = -0.5 \, V \), \( t_{\text{pause}} = 100 \, \mu s \).
7. Explicit test of the accessible number of states

Supplementary Figure S9: Distinct conductance states. Increase of conductance over 10 pulses with error bars. Maximum standard deviation during a read pulse was 0.31 µA. Settings: \( t_{\text{write}} = 0.1 \, \text{s} \), \( V_{\text{write}} = -0.7 \, \text{V} \), \( t_{\text{read}} = 0.1 \, \text{s} \), \( V_{\text{read}} = -0.1 \, \text{V} \), \( t_{\text{pause}} = 0.1 \, \text{s} \). The measurement error stems from noise and discharging during read out pulses.

According to van de Burgt et al. [4] at least 100 distinct conductive states for synaptic devices are required to work adequate as a synaptic weight in a DNN. Additionally, Yu et al. simulated that the accuracy of their DNN starts to saturate at a state number of 128[9]. For a qualitative estimation of the possible states, we assume that a separation of the conductance level by two times the maximum measured standard deviation is sufficient for distinguishability. Fig. S9 shows a measurement of 10 pulses together with the standard deviation. The maximum standard deviation was 0.31 µA. As can be calculated from Fig. 2a in the main manuscript, the maximum current realized by switching was 0.2 mA (Conductance * Voltage = 392 µS * 0.5 V). Hence, the estimated number of distinguishable conductance states calculates to 322 (Calculation: 0.2 mA/(2x0.31 µA) ). Please note that this is an overestimation due to the different read-out voltages used between Figure. 2a and Figure S9. Higher voltages could lead to a higher standard deviation. Nevertheless, 322 states are 3 times more than actually needed. Further studies in decreasing noise and reducing pulse times can increase this number.
8. Conductive change parameters

Supplementary Figure S10: Write time/voltage sweep measurements: Circuit as in Fig. S5. All measurements were performed with different devices. a) Changing the write pulse duration while keeping the other parameters constant at $V_{\text{write}} = -0.8\, \text{V}$, $t_{\text{read}} = 5\, \text{ms}$, $V_{\text{read}} = -0.1\, \text{V}$, $t_{\text{pause}} = 100\, \mu\text{s}$. b) Changing the write voltage while keeping the other parameters constant at $t_{\text{write}} = 100\, \mu\text{s}$, $t_{\text{read}} = 5\, \text{ms}$, $V_{\text{read}} = -1\, \text{mV}$, $t_{\text{pause}} = 100\, \mu\text{s}$.

Supplementary Figure S11: Down writing sweep: a) Changing the voltage of writing after pulse 500. Other parameters remain constant. Settings: $t_{\text{write}} = 5\, \text{ms}$, $V_{\text{write, up}} = -1.2\, \text{V}$, $t_{\text{read}} = 10\, \text{ms}$, $V_{\text{read}} = -0.1\, \text{V}$, $t_{\text{pause}} = 100\, \mu\text{s}$. b) Exemplary raw data before processing. Top plot shows the applied pulse scheme during the measurement. Bottom plot is the measured current response over time. Settings: $t_{\text{write}} = 0.1\, \text{s}$, $V_{\text{write}} = -0.7\, \text{V}$, $t_{\text{read}} = 0.1\, \text{s}$, $V_{\text{read}} = -0.1\, \text{V}$, $t_{\text{pause}} = 0.1\, \text{s}$.
9. PPF/PTP Measurement

**Supplementary Figure S12**: Paired-Pulse facilitation measurement. Two equal gate pulses with -0.6V_DG separated by Δt are applied at the EGOT while a constant drain voltage of -0.1V_DS is present. The ratio of the maximum current responses A2/A1 between the first and second pulse is plotted over the time separation. A double exponential decay is fitted to the data. a) Pulse width t_p of 10 ms and b) pulse width t_p of 100 ms. Each measurement is acquired ten times.

Paired pulse facilitation (PPF) is a short-term plasticity effect in biological synapses and lasts between milliseconds to few minutes [10]. Two pre-synaptic action potentials separated by Δt in time lead to membrane potential changes at the post-synaptic side with corresponding amplitudes A1 & A2 due to ion penetration into the membrane. An increase of A2 with respect to A1 is called PPF. The opposite process, where A2 decreases, is called paired-pulse depression. By increasing the time delay Δt of the second pulse, the correlation between these two pulses becomes weaker. In some synapses the function of A2/A1(Δt) follows a double exponential decay according to

$$\frac{A_2}{A_1} = C_1 e^{-\Delta t/\tau_1} + C_2 e^{-\Delta t/\tau_2} + 1. \quad (1)$$

Often, a distinction of the two decays is not possible and a single exponential fit is sufficient. The decays originate from the ion diffusion out of the post-synapse back into the synaptic cleft and a relaxation of the neurotransmitter density in the cleft, if no action potential is present at the pre-synaptic side[10]. Similar holds for the EGOT devices. For shorter time delays, more ions accumulate in the channel. Hence, a higher current response for the second pulse is observed. Increasing the time gap allows the ions to diffuse back into the electrolyte and de-dope the channel [11]. We were able to measure similar decay behaviour as in human synapses. For the 10 ms pulse duration, (see Supplementary Figure S12a) comparable timescales to the biological synapses are achieved with \(\tau_1 = 3.7\) ms and \(\tau_2 = 92.1\) ms.
[10, 12]. The time constants themselves depend on the pulse durations. For instance, Fig. S12b represents a measurement with a 100ms pulse duration and increased time constants $\tau_1 = 0.17s$ and $\tau_2 = 1.64s$.

A train of pulses can facilitate the information transport over a synapse even further. This synaptic plasticity effect is called post tetanic potentiation (PTP) [12] and was already observed in a memristive device reported by Liu et al. [13]. Connecting the drain and gate electrodes during a pulse train of 100 pulses with a pulse length of 100 ms and a bias of -0.7 V lead to an overall increased current response (see Fig. S13). The time between the pulses (100 ms) is not sufficient for the ions to fully relax back into the electrolyte. Hence, an accumulation of the ions in the channel occurs.

Supplementary Figure S13: Post-tetanic-potentiation measurement. The gate and the drain contacts are connected and a train of 100 input pulses with a bias of -0.7 V and 100 ms duration is applied. Between each pulse, a 100 ms pause with 0 V at the input is present. An increasing current response with higher pulse number was measured because of the ion accumulation in the channel.
10. Pavlov's experiment

**Supplementary Figure S14: Electrical version of Pavlov's dog.** a) The measurement is subdivided into four phases similar to the classical conditioning experiment. In the first phase only the food input is applied with a non-zero response of the salivation current, followed by merely bell input signals with no significant response. During the third phase, both inputs are activated simultaneously and an increasing response can be observed corresponding to learning. In the last phase, the bell signal is now sufficient to create a non-zero response. The current decrease is referred to unlearning mechanism. b) Electrical circuit of the experiment. Pulse duration and pause time each are 1 s. Food signal 5 V. Bell signal -0.6 V.

The well-known classical conditioning experiment performed by Pavlov was one of the first concepts of learning behaviour. The experiment had the following sequence.

Food is offered to a dog, which is used as an unconditioned stimulus (UCS). The natural response to food is salivation, an unconditioned response (UCR). Ringing a bell does not have any effect on the dog in the beginning and serves as a neutral stimulus (NS). Pavlov trained his dog by presenting food (UCS) together with ringing the bell (NS). After a while, the dog associates the ringing bell with getting food, thereby the NS is becoming a conditioned stimulus (CS). The salivation is now a conditioned response (CR) to the CS. If the dog only hears the bell (CS) without receiving food (UCS) for a while, the association will disappear and the bell is turning back into a NS [14].

We were able to realize this learning experiment with an electrical circuit including our EGOT device (see Fig. S14a). It contains two inputs as representatives of the bell and food from the original experiment. The measured current response mimics the salivation of the dog. Applying a food signal (UCS) leads to a current flow over the resistor (UCR) and simultaneously closes the switch. A bell signal (NS) produces a drain source current over the EGOT channel depending on the conductance state. Changing this state is only possible if a food signal is present and if consequently the switch is closed. Then the bell signal can force ions from the electrolyte to penetrate the channel and increase its conductance. This phase corresponds to the association process where the bell becomes a CS. The measurement run is depicted in Fig. S14b. It shows a current response in the case of solely food signals. During the first bell signals (NS), no current response was monitored. Synchronous food and bell signals
show a steady increase of the current, which is corresponding to the learning phase, followed by a decreasing response when solely a bell signal is applied. The association becomes weaker over time and the food signal goes back to a NS.

The single-input single-output (SISO) configuration (see Fig. 4a) shows the feasibility to send information over a chain of EGOTs. This setup reflects an information transfer through a neuron cell over the input and output synapses. Figure S15 shows the response during an input signal sequence (see inset Figure S15a). Both synapses exhibit an increase in their conductance (see Figure S15a) due to ion accumulation in their channels. Additionally, higher output responses are measurable whilst keeping the input train present (see Figure S15b). This behaviour can be understood as a realization of learning reminiscent to biological synapses. The information transfer over our electrical neuron is facilitated during the usage. The voltage drop over the second EGOT is increasing (see Fig. S15c) caused by a reduced resistance ratio between the first EGOT and the parallel input resistance of the oscilloscope together with the second EGOT.

Supplementary Figure S15: Single-Input Single-Output measurement. Two EGOTs in series with their gate and drain contacts connected (see Fig. 4a). a) Output current, b) voltage drop over the second EGOT and c) resistance of the EGOTs over 100 applied pulses. The pulse sequence is represented in the inset of c). Input settings: $t_{ON} = 10 \text{ ms}$; $t_{OFF} = 1.5 \text{ ms}$; $V_{ON} = -0.7 \text{ V}$; $V_{OFF} = 0 \text{ V}$. 
12. Single-Input Multiple-Output

On the other hand, the single-input multiple-output (SIMO) configuration allows verifying the possibility of an interconnection at the output side similar to the neuron cells at the axon terminals, which can transmit their electrical impulse to multiple post-neurons. The SIMO system consists of one input synapse and two output synapses (see Fig. 4a). The results of the output currents are plotted depending on the number of input pulses (see Fehler! Verweisquelle konnte nicht gefunden werden.). Our measurements show that input signals can be distributed over multiple EGOTs while both outputs exhibit the synaptic strength increase due to the ion accumulation. Since our devices are not industrially fabricated, the output current responses differ with respect to the absolute value. Whereas the relative current change is similar for both outputs. Enlarging the number of outputs would be the next step to achieve a comparison to the biological neurons.

Supplementary Figure S16: Single-Input Multiple-Output measurement. One input EGOT in series with two parallel output EGOTs. Each EGOT has its gate and drain contacts connected (See Fig. 2c). a,b) Normalized current response on 1. Output (a) and 2. Output (b) over 200 applied pulses. The pulse sequence is represented in the inset of c). Input settings: t_{ON} = 10ms; t_{OFF} = 1.5ms; V_{ON} = -0.6V; V_{OFF} = 0V.
Supplementary Figure S17: Multiple-Input Single-Output Setup. It shows the wiring of Fig. 4. a) The chip (grey) with the three EGOTs on a chip carrier. The pins and the electrodes are connected via gold wires and silver paste. For visibility reasons scaling is not considered b) The breakout box with BNC outlets. The inputs are generated by wave generators and the final current is translated into a voltage with a transimpedance amplifier. Voltages are measured by an oscilloscope. The numbers correspond to the ones in Fig. 4 (S1-S3).

The interconnection is done by wire bonding of the transistors onto a chip carrier. A picture of a single transistor is shown in Figure S1. The actual connections then are done by BNC cables externally. Figure S17 shows exemplary the wiring for the MISO measurement (see Figure 4). We agree that for highly integrated networks the way to connect the individual transistors is critical, but not the focus of the current work. We believe that a high interconnection with multiple devices could be designed by e-beam lithography combined with an ion gel.
References


