Supporting Information for

Statistical study on the Schottky barrier reduction of tunneling contacts to CVD synthesized MoS$_2$

Seunghyun Lee$^{†,§,*}$, Alvin Tang$^{†,§}$, Shaul Aloni$^‡$, H. -S. Philip Wong$^†$

$^†$Department of Electrical Engineering and Stanford SystemX Alliance, Stanford University, Stanford, California 94305, USA.

$^‡$The Molecular Foundry, Lawrence Berkeley National Laboratory, Berkeley, California 94720, USA

§ These authors contributed equally to this work.

*Corresponding author. Electronic mail: seansl@stanford.edu

1. Band alignment of MoS$_2$ and Ta$_2$O$_5$

![Band alignment of MoS$_2$ and Ta$_2$O$_5$](image)

Figure S1. Band alignment of MoS$_2$ and Ta$_2$O$_5$. $^{1,2}$
2. Synthesis of Large Area Multilayer MoS$_2$

2 cm × 2.5 cm pieces of 285 nm SiO$_2$/Si were RCA cleaned (1:1:5 NH$_4$OH/H$_2$O$_2$/H$_2$O bath followed by 1:1:5 HCl/H$_2$O$_2$/H$_2$O bath) and then O$_2$ plasma cleaned. Individual pieces were then loaded into a 2 inch CVD furnace quartz tube; substrates were placed face down on top of a MoO$_3$ quartz boat filled with ~5-6 mg of MoO$_3$ powder (Alfa Aesar, Puratronic 99.9995% purity) at the center of the tube. ~100 mg of Sulfur powder (Alfa Aesar, Puratronic 99.999% purity) was placed upstream ~27 cm (10.5 in.) away from the center. A schematic of the CVD furnace set up is shown below (Figure S1.):

![Figure S1. Schematic of the CVD furnace set up.](image)

Before each growth, the system was filled with Ar gas (Ar flow on, pump off) and subsequently purged (Ar flow off, pump on) a total of ten times before setting the ambient condition to ATM pressure (760 torr) at 50 sccm Ar flow rate. The furnace was first ramped from room temperature to 500°C in 30 minutes and then held at 500°C for 20 minutes. Temperature was then ramped to 740°C in 20 minutes and then held at 740°C for 30 minutes before cooling slowly to room temperature. A schematic of the MoS$_2$ growth temperature profile is shown below (Figure S2.):
**3. Fabrication Process**

40 nm HfO$_2$ was first deposited by ALD onto Si substrates at 200°C. For each ALD cycle, tetrakis (dimethylamido) hafnium precursor (raised to 75°C) was pulsed into the ALD chamber for 0.3 s followed by an H$_2$O pulse for 0.015 s. As-grown MoS$_2$ released from 285 nm SiO$_2$/Si in an HF bath was then transferred onto the HfO$_2$/ Si substrates. Subsequently, a Ta$_2$O$_5$ layer, varying from 0-5 nm, was deposited by ALD on top of this stack at 200°C. For each ALD cycle, tris ((ethylmethylamido)tert-butylamido) tantalum (V) precursor (raised to 120°C) was pulsed into the ALD chamber for 0.3 s followed by an H$_2$O pulse for 0.015 s. Then Ti/ Au contacts (3 nm/ 30 nm) were formed via lift off and final patterning was done using CF$_4$ gas etching at RF power of 500 W and a chamber pressure of 150 mT for 1 minute.

![Graph](image-url)  

**Figure S3.** Temperature vs. time profile for multilayer MoS$_2$ growth.
4. Pinning Factor

![Figure S4](image)

**Figure S4.** (a) Arrhenius plot for extracting the Pt / MoS$_2$ contact Schottky barrier. (b) Schottky barrier height as a function of metal work function. The Schottky barrier height for Ti / MoS$_2$ contacts is from Figure 3c in the main text.

We measured the Schottky barrier heights for another metal (Pt) contacted to MoS$_2$ and compared it with Ti contacts to extract the pinning factor. From the temperature dependent measurement, the average Schottky barrier height for Ti / MoS$_2$ contacts and Pt / MoS$_2$ contacts was found to be 95 meV and 237 meV, respectively. Thus, the pinning factor $S$ extracted from the slope was found to be $S=0.107$ as shown in Figure S4. The value was slightly smaller than the $S=0.113$ value extracted from the trend line shown in another article$^3$. 
5. Effect of Ta$_2$O$_5$ layer on the Drive Current and Threshold Voltage

**Figure S5.** MoS$_2$ transistor drive current increase when comparing without (a) and with (b) the Ta$_2$O$_5$ tunneling insulator.

**Figure S6.** Extraction of the threshold voltage ($V_{Th}$) and increased drive current for MoS$_2$ transistors without (a) and with (b) the Ta$_2$O$_5$ tunneling insulator.

**References**