Cascading wafer-scale integrated graphene complementary inverters under ambient conditions

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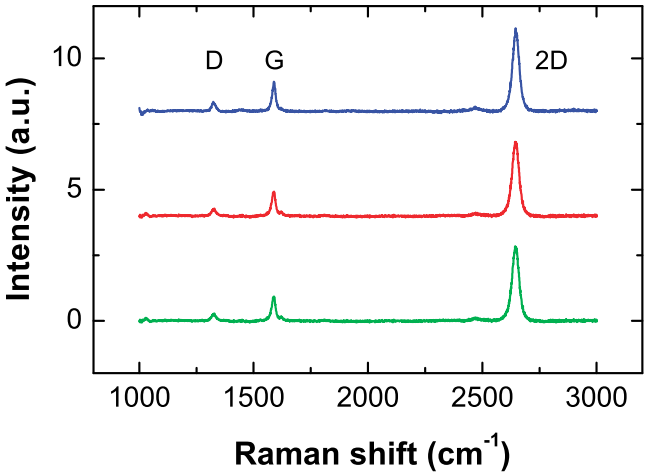

Figure S1: Raman spectra of typical graphene films used in this study. The G/2D peak ratio suggests the presence of primarily monolayer graphene, while the small integrated D/G ratio (< 0.2) implies relatively good quality of graphene grown by chemical vapor deposition (CVD).[1]

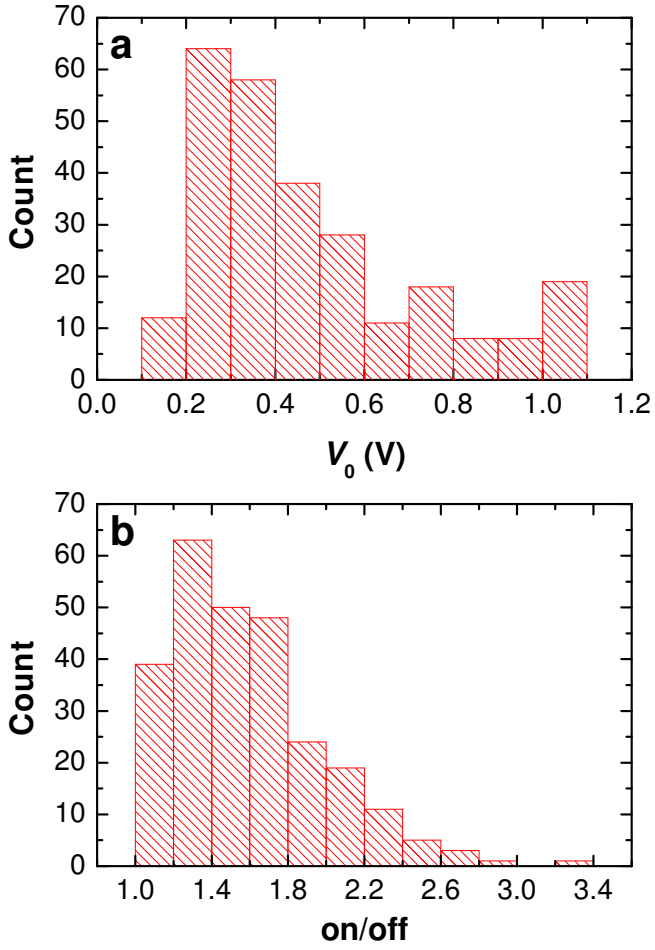

Figure S2: Statistics on 264 fabricated graphene FETs incorporated in complementary inverters. Measurements were performed under ambient conditions. a) Histogram of the Dirac point voltage V_0 of the top gate. The average value of the Dirac voltage is $V_0 = 0.43$ V. b) Histogram of the on/off ratio of the drain current I_D obtained from the transfer curves I_D vs. V_G in the range $|V_G| < 1$ V (see Figure S3). The average on/off ratio is 1.58. High-gain inverters were comprised of symmetric FETs with on/off > 2.

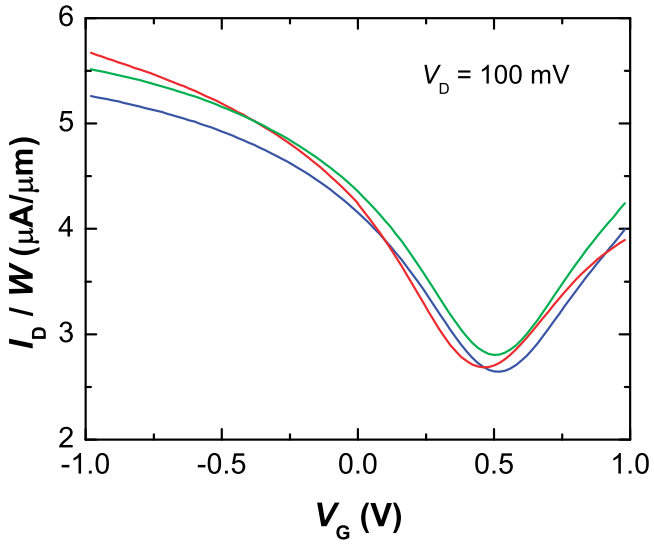

Figure S3: Transfer curves I_D vs. V_G of typical top-gated graphene FETs ($L = 2$ μm and $W = 20$ μm) with on/off ~ 2.

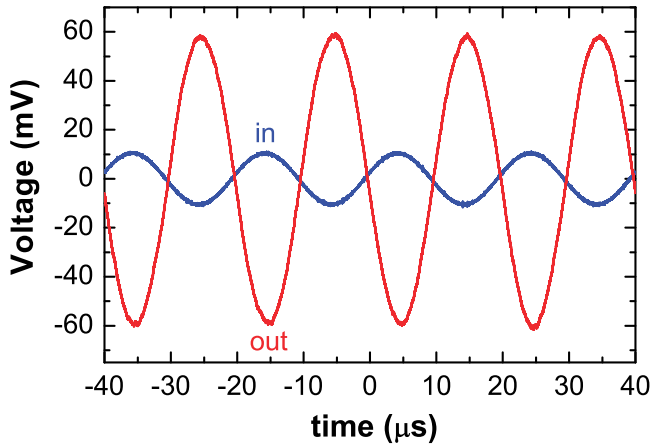

Figure S4: AC components of the input and output voltage signals measured in a graphene inverter in air ambient at a frequency $f = 50$ kHz for $V_{DD} = 2.5$ V. The voltage gain is $A_v = -5.3$. The DC components of the signals are $V_{IN} = 1.47$ V and $V_{OUT} = 1.33$ V.

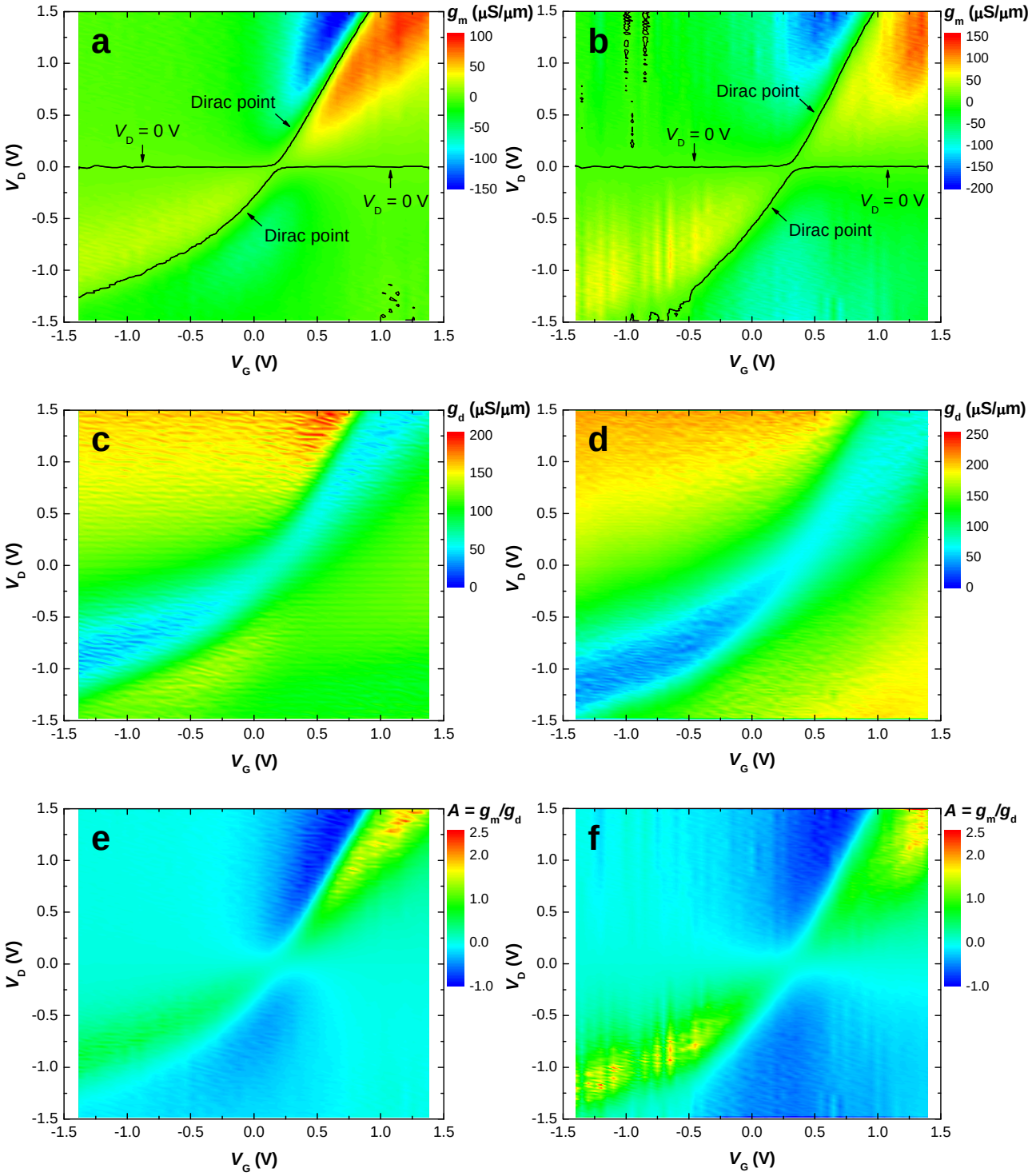

Figure S5: Typical small-signal parameters of the fabricated FETs ($L = 2$ μm and $W = 20$ μm) in air. a)-b) Transconductance g_m. c)-d) Output conductance g_d. e)-f) Intrinsic voltage gain $A = g_\mathrm{m}/g_\mathrm{d}$. Parameters of two different samples a)-c)-e) and b)-d)-f) are plotted as functions of the DC biasing, i.e., gate voltage V_G and drain voltage V_D. Zero-transconductance lines are shown in the transconductance plots a)-b). The horizontal lines correspond to a zero-biasing condition ($V_\mathrm{D} = 0$) while diagonal lines correspond to the Dirac point. The parameters are given "as measured", i.e., without subtracting the parasitic resistances.

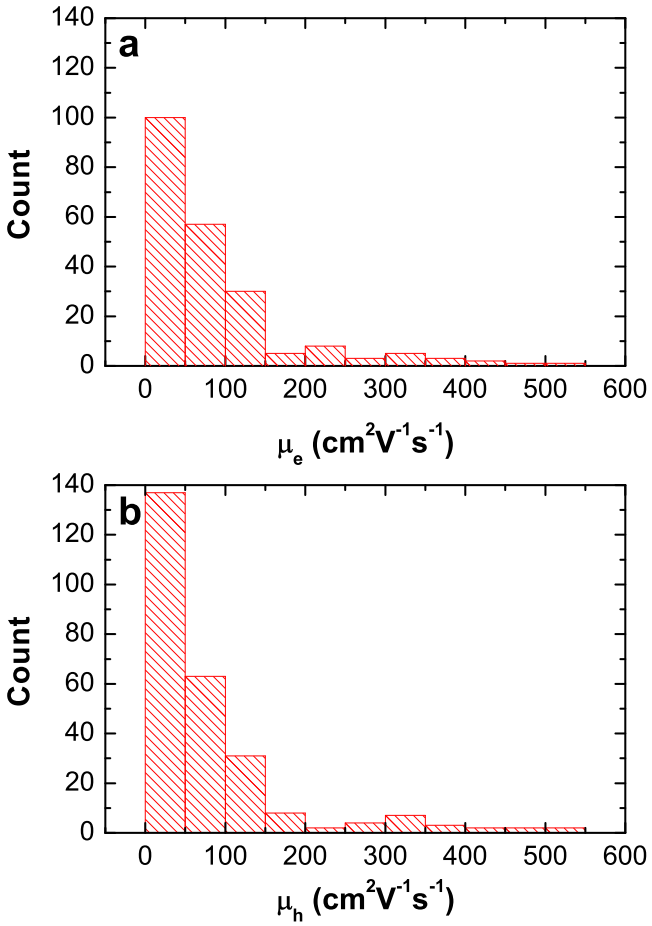

Figure S6: Statistics on the extrinsic mobility (without subtracting contact resistance) of the fabricated graphene FETs incorporated in complementary inverters. Measurements were performed under ambient conditions. a) Histogram of the extrinsic electron mobility μ_{e} of 215 FETs. b) Histogram of the extrinsic hole mobility μ_{h} of 261 FETs. The extrinsic carrier mobility $\mu \sim 300$ cm^{2}V^{-1}s^{-1} translates into intrinsic carrier mobility $\mu_{\mathrm{in}} \sim 1000$ cm^{2}V^{-1}s^{-1} after extraction of the contact resistance $R_{\mathrm{c}} \sim 450\ \Omega$ (9 k$\Omega \cdot \mu$m).

Inverters with larger Dirac voltages

We also investigated inverters with larger Dirac voltages ($V_0 > 0.2$ V) in which signal matching was possible only at the expense of a gain loss. In such samples it was necessary to shift the Dirac point back to zero and hence eliminate mismatch between the input and output signals at the highest-gain point. We found that this could be achieved by keeping such samples in high vacuum

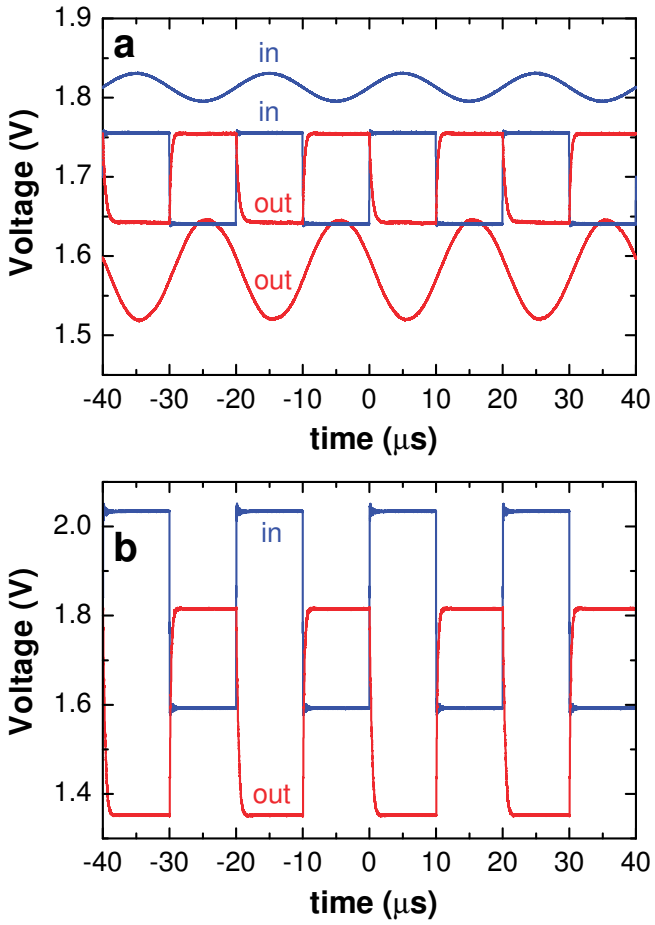

Figure S7: Analog and digital waveforms measured at the input and output of a typical graphene inverter with $V_0 = 0.23$ V under ambient conditions at a voltage supply $V_{DD} = 2.5$ V and frequency $f = 50$ kHz. a) Sine waveform signals measured at the highest-gain point at which there is a mismatch of $V_0 = 0.23$ V between the DC components of the signals. The amplitude of the output sine wave is 3.5 times larger than the amplitude of the input sine wave, hence $A_v = -3.5$. Digital waveforms were measured at the DC operating point at which there is no in/out DC signal mismatch. The largest input voltage swing $V_{in,p-p} = 0.12$ V at which the signals are matched is used. b) Digital waveform signals measured at the highest-gain point. The digital voltage swing ($V_{in,p-p} = 0.48$ V) is much larger than in the case when the inverters are operated with matched signals.

(at a pressure $\sim 10^{-5}$ mbar for ~ 1 day prior to measurements). Although the graphene channel is completely covered by the gate, diffusion of molecules at the gate/graphene interface cannot be prevented, which leads to the desorption of ambient impurities from graphene in vacuum. After $V_0 = 0$ was reached, such samples were measured at a low pressure of ~ 200 mbar which was low enough to keep the Dirac point at zero. Apart from maintaining the Dirac point at zero and slightly reducing the voltage gain (by $\sim 18\%$), testing at low pressure was not found to have any other influence on device operation (see Supporting Figures S6–S8). Both in air and at low pressure, over-unity voltage gain is preserved when the inverters are operated in the AC mode.

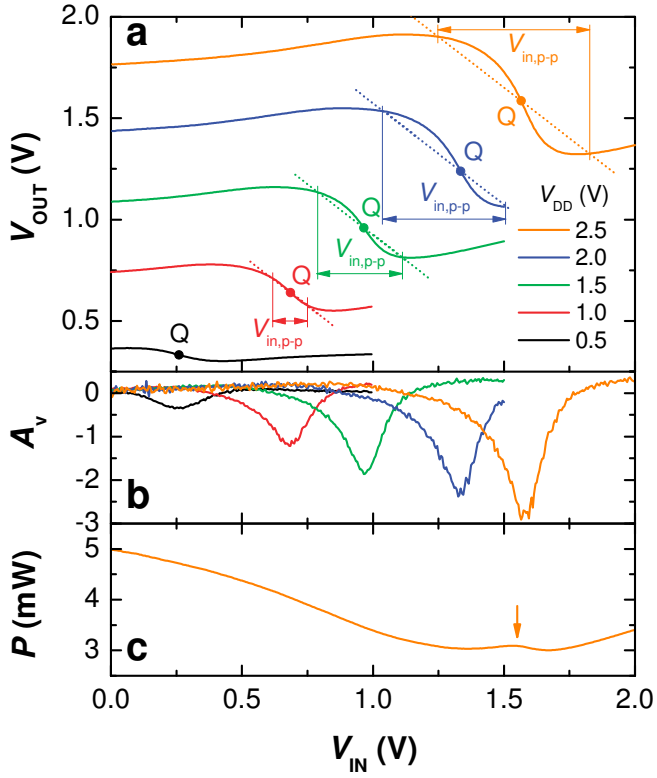

Figure S8: DC characteristics of a graphene inverter with $V_0 = 0.23$ V at a pressure $p = 200$ mbar.. a) Transfer curves of an inverter at different supply voltages. The highest-gain point at each supply voltage is denoted by Q. The maximum input voltage swing $V_{\mathrm{in,p-p}}$ at which input and output signals are matched ($V_{\mathrm{out,p-p}} = V_{\mathrm{in,p-p}}$) is determined by the intersections between the transfer curve and a unity gain line (slope of -1) passing through Q. b) The DC voltage gain A_{v} of the same inverter at different supply voltages. c) Power dissipation of the same graphene inverter at $V_{\mathrm{DD}} = 2.5$ V. The arrow represents the local maximum of dissipated power at the Q point, similar to Si inverter technology.

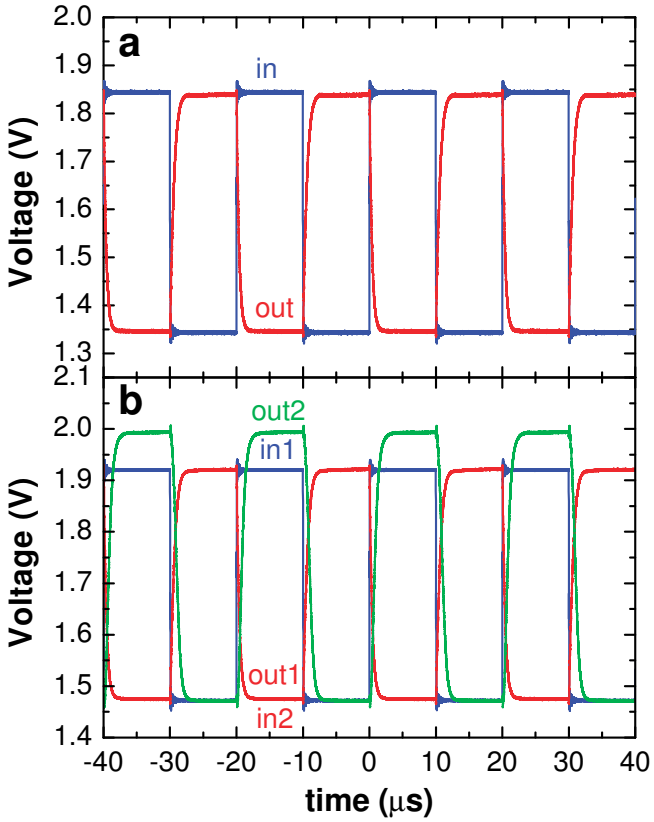

Figure S9: Matched input and output signals measured in a graphene inverter with $V_0 = 0.23$ V at a frequency $f = 50$ kHz and pressure $p = 200$ mbar. a) Digital waveforms in the case of a maximum input voltage swing $V_{\text{in,p-p}} = 0.5$ V at which in/out signals are matched at $V_{\text{DD}} = 2.5$ V. b) Digital waveforms measured in a cascade connection of two graphene inverters (connected as in Figure 1c). The supply voltage is $V_{\text{DD}} = 2.5$ V.

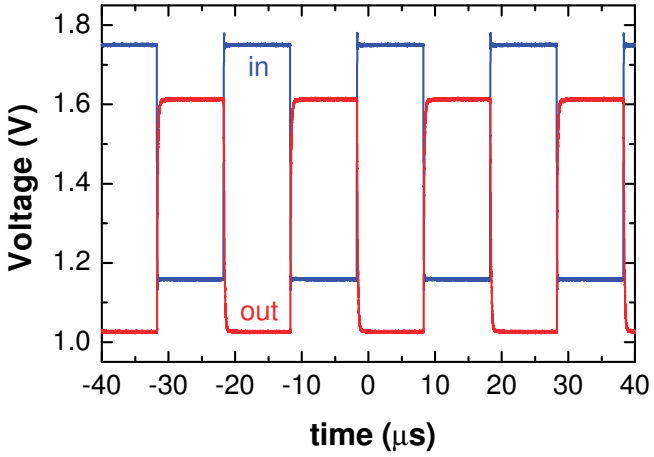

Figure S10: Digital waveforms measured at the input and output of the graphene inverter from Figure 2 in air at a voltage supply $V_{\text{DD}} = 2.5$ V and frequency $f = 50$ kHz. The waveforms were measured at the highest-gain point at which there is a mismatch of $V_0 = 0.11$ V between the DC components of the signals.

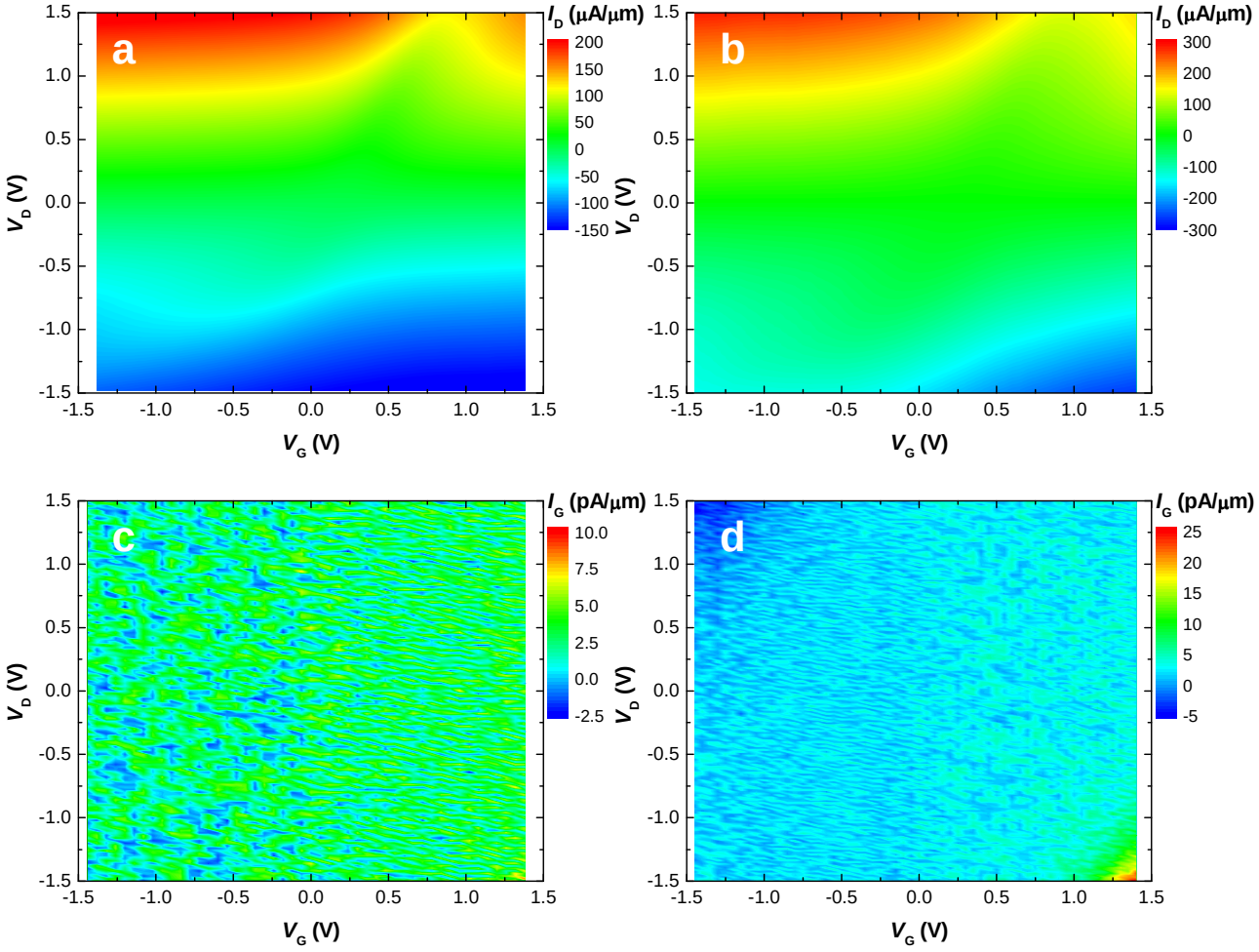

Figure S11: Drain current I_D and gate current I_G as functions of the DC biasing of two typical fabricated FETs ($L = 2$ μm and $W = 20$ μm) a)-c) and b)-d) in air. The largest gate leakage current is obtained for largest $|V_{DG}|$, i.e., in the upper-left and bottom-right corners of the plots c)-d), while fabricated inverters operate with matched in/out voltages, i.e., with $V_{DG} \approx 0$ in the upper-right corner of the plots.

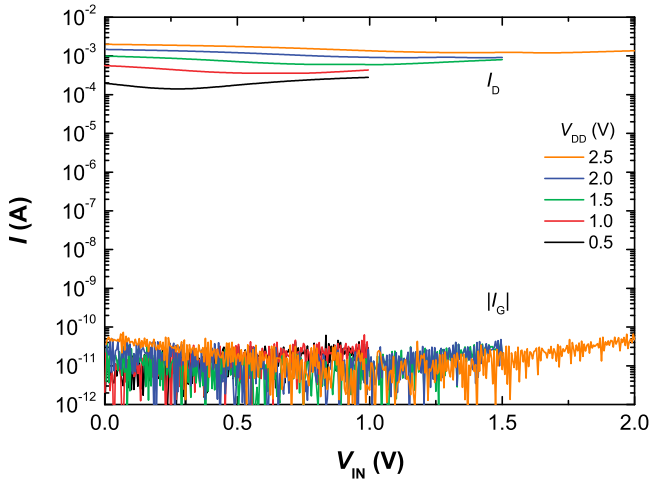

Figure S12: Drain current I_{D} and gate current I_{G} of the sample shown in Figure S8 ($L = 2\ \mu$m and $W = 20\ \mu$m).

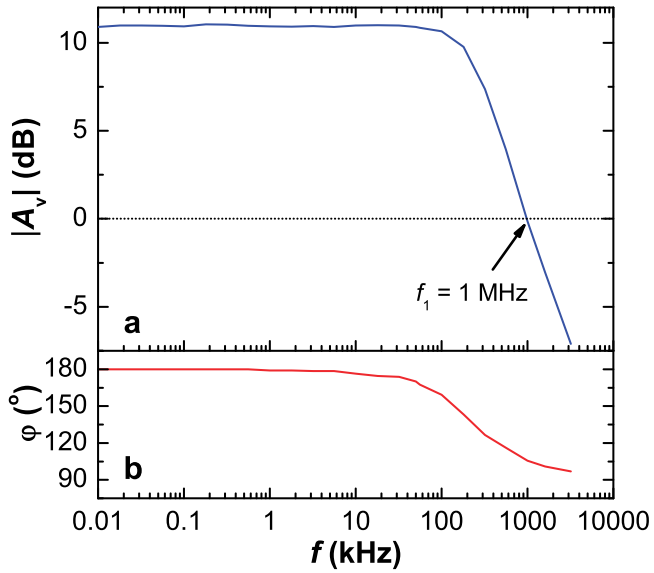

Figure S13: Frequency response $A_{\mathrm{v}} = |A_{\mathrm{v}}|\angle\varphi$ of a typical inverter for $V_{\mathrm{DD}} = 2.5$ V. a) Magnitude $|A_{\mathrm{v}}(f)|$ of the voltage gain. b) Phase shift $\varphi(f)$ between output and input signals introduced by the inverter. The -3 dB bandwidth of the inverter is ~ 270 kHz, while the unity-gain frequency (the highest frequency at which signal amplification is still possible) is $f_1 = 1$ MHz. The bandwidth is limited by the output conductance of the inverters ($g_{\mathrm{out}} \sim 1$ mS) and parasitic capacitance of the cables ($C_{\mathrm{c}} \sim 0.6$ nF) to $f_{-3\,\mathrm{dB}} = g_{\mathrm{out}}/(2\pi C_{\mathrm{c}}) \approx 270$ kHz.[2]

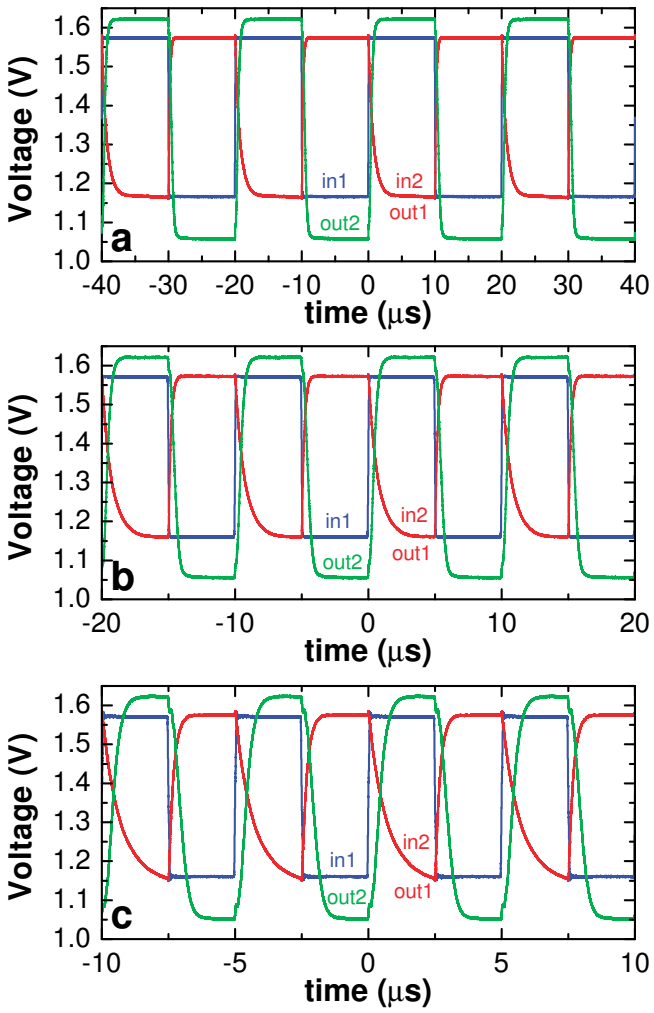

Figure S14: Matched input and output digital signals measured in a cascade connection of two graphene inverters (connected as in Figure 1c) under ambient conditions at a supply voltage $V_{DD} =$ 2.5 V and frequency a) $f = 50$ kHz, b) $f = 100$ kHz, and c) $f = 200$ kHz.

References

(1) Wood, J. D.; Schmucker, S. W.; Lyons, A. S.; Pop, E.; Lyding, J. W. *Nano Lett.* **2011**, *11*, 4547–4554.

(2) Guerriero, E.; Polloni, L.; Rizzi, L. G.; Bianchi, M.; Mondello, G.; Sordan, R. *Small* **2012**, *8*, 357–361.