# Supporting Materials for

Multilevel Resistive Switching in Planar Graphene/$SiO_2$ Nanogap Structures

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**Imaging at the broken gap region**

A broken gap region formed after forming process was observed clearly. The SEM images of a device before and after the forming process, shown in Figure S1 (a) and (b), also clearly demonstrate a crack formation across the NG stripe. To investigate the detail of the gap region, we carried out plasma etching. The etching conditions are as follows: temperature: ~350 °C; reaction gas: pure hydrogen; pressure: ~0.27 Torr; RF power: ~120 W. It etched the NG film away but has nothing to do with the $SiO_2$ substrate. The AFM and SEM image, showing in Figure S1 (c) and (d), indicates substantial damage to the $SiO_2$ substrate in the nanogap region.

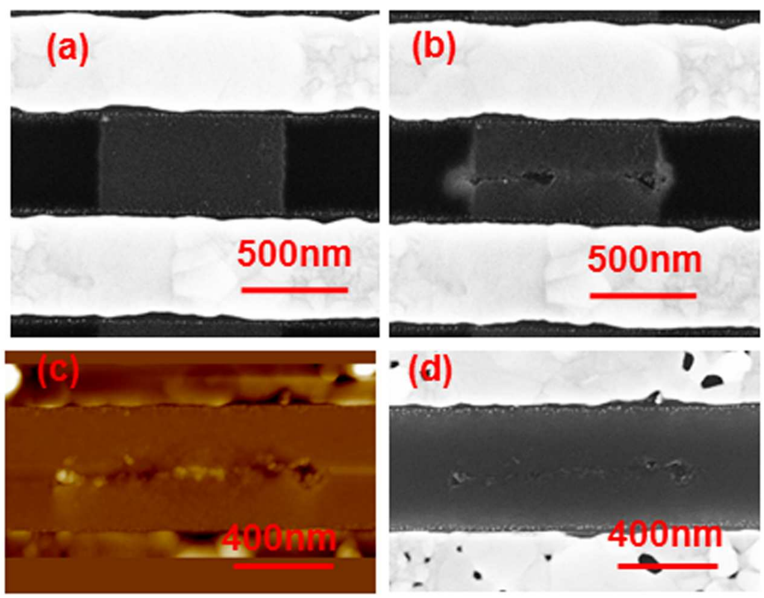


Figure S1. (a and b) SEM image of a device before and after forming process. The AFM (c) and SEM (d) image of the gap region after removing the nanographene film by PECVD etching shows a substantial damage to the $SiO_2$ substrate in the gap region.

**The Forming process of the two-terminal resistance switching devices with different lengths (l) and widths (w) nanographene stripe**

The break-down *I-V* curves of the two-terminal resistance switching devices with different lengths (*l*) and widths (*w*) were shown in Figure S2 (a) and (c). Figure S2 (b) and (d) shows that the break voltage linearly depends on the length *l*, while the break current linearly depends on the width *w*. These observations are evidences for Joule-heat generated by the applied bias voltage. The Joule heat *Q* generated by applied voltage should be enough to break-down the NG films, which can be expressed as the following equation (1)[1]

$$Q \propto C \cdot m \cdot T_{break} = C \cdot \rho \cdot l \cdot w \cdot t \cdot T_{break} \tag{1}$$

where C and ρ are the specific heat and density of the NG films, respectively. According to Joule's low, we can get the equation (2)

$$Q = \frac{V_{break}^2}{R}\tau = \frac{V_{break}^2 \cdot w \cdot t \cdot \tau}{\gamma \cdot l} \tag{2}$$

where τ and γ are the time and resistivity of the NG films, respectively. Combining equation (1) and (2), we obtain equation (3)

$$V_{break} \propto \sqrt{\frac{C \cdot \rho \cdot \gamma \cdot T_{break}}{\tau}} l = Al \tag{3}$$

$$Q = I_{break}^2 \cdot R \cdot \tau = \frac{I_{break}^2 \cdot \gamma \cdot l \cdot \tau}{w \cdot t} \tag{4}$$

Combining equation (1) and (4), we obtain equation (5)

$$I_{break} \propto \sqrt{\frac{C \cdot \rho \cdot T_{break}}{\gamma}} wt = Bwt \tag{5}$$

where A and B are independent of geometric parameters of the devices. Thus, $V_{\mathrm{break}}$ linearly depends on the *l* and is independent of *w* and *t*, whereas, $I_{\mathrm{break}}$ is independent of *l* and linearly depends on *w* and *t*, which agree with our experimental results.

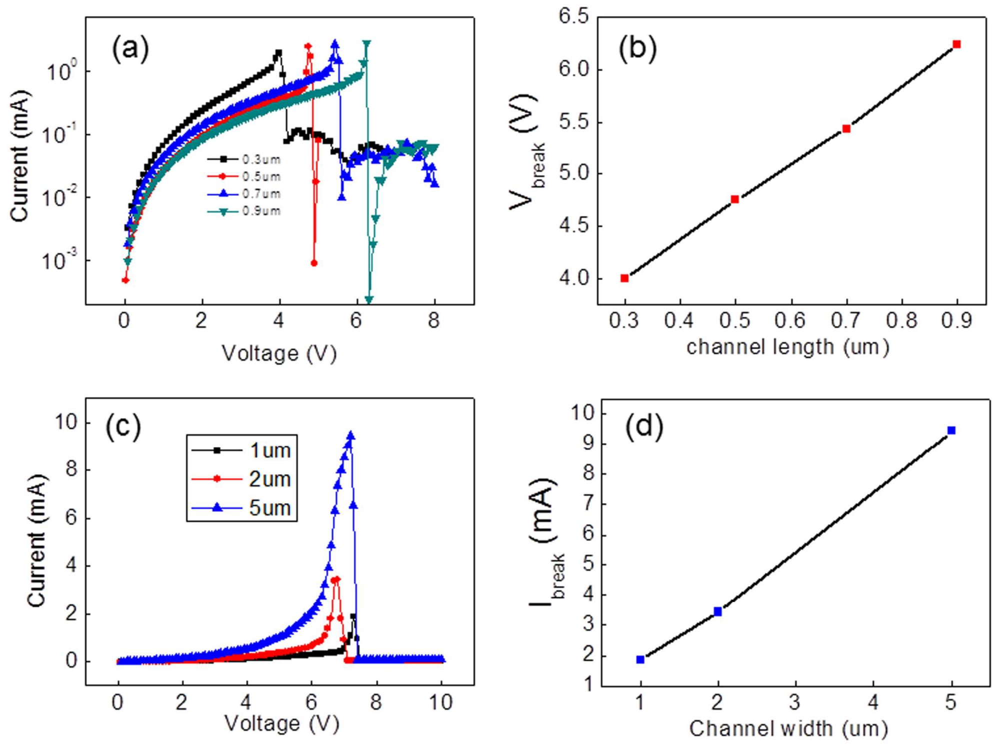


Figure S2. (a) The break *I-V* curves of the devices with different length l and (b) the break voltage linearly depends on the length l. (c) The break *I-V* curves of the devices with different width w and (d) the break current linearly depends on the device width.

**The *I-V* curves fitting by Simmons' equation**

The tunneling conduction in our experiment was attributed to silicon nanocrystallites embedded in the insulating matrix formed by the forming process. The tunneling current density (J) under intermediate-voltage bias (V< $\varphi_B$ /e) was expressed by the Simmons' equation as the following equation2-4:

$$J = \frac{I}{A} = (\frac{q}{4\pi^2 \hbar d^2})\{(\varphi_B - qV/2)\exp[-\frac{2d(2m)^{1/2}}{\hbar} \times (\varphi_B - qV/2)^{1/2}]$$
$$-(\varphi_B + qV/2)\exp[-\frac{2d(2m)^{1/2}}{\hbar} \times (\varphi_B + qV/2)^{1/2}]\} \qquad (1)$$

where A is the tunneling area, d is the tunneling distance, m is mass of electron, q is charge of electron, and $\hbar$ is reduced Planck's constant. The I-V curve of the ON state under intermediate-voltage bias at 200K, which could not induce the conduction switching, were well fitted by Eq. (1) to adjusting parameters $\varphi_B$, A, and d. The fitting parameters $\varphi_B$, A, and d of ON state are 0.56±0.005 eV, 567.5±0.1 $nm^2$, and 0.77±0.005 nm, respectively. The tunneling distance d indicated that the silicon nanocrystallites formed in the forming process were arranged in a nearly continuous conductive pathway embedded in $SiO_2$ matrix at ON state. We can get the radius of the nanocrystalline Si filament was ~ 13.4 nm when assume the silicon nanocrystalline clusters were spherical shape.

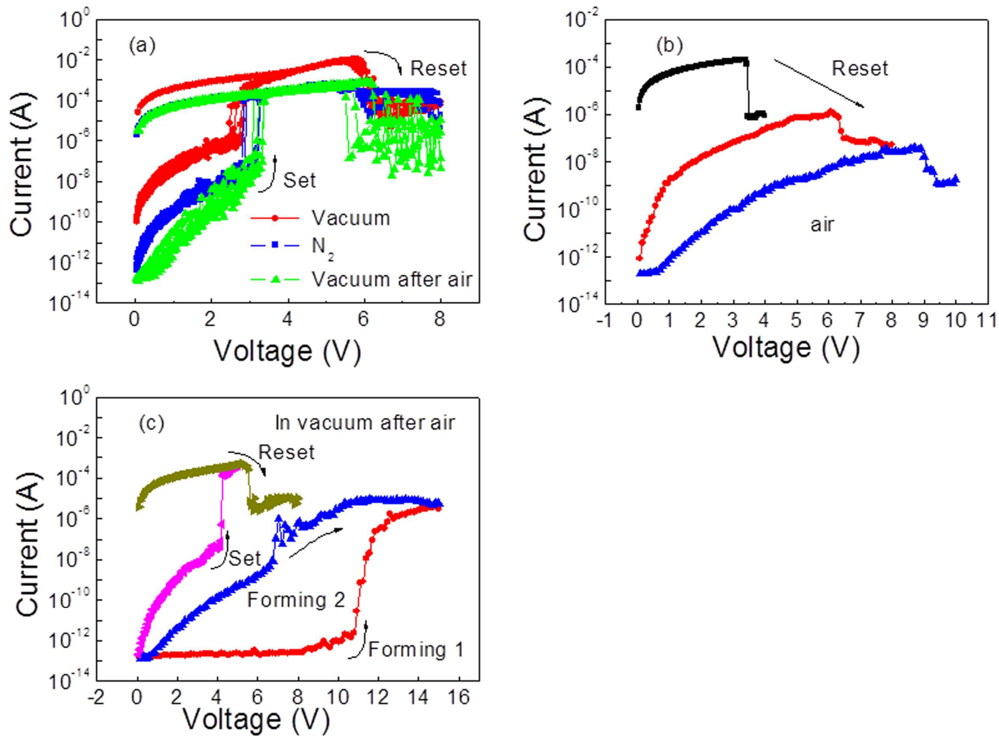


Figure S3. (a) The set and reset *I-V* curves of the device in vacuum and nitrogen measure conditions. (b) The reset *I-V* curves obtained only in the atmosphere measure condition, while the set process cannot happen. (c) A new forming process were happened when measurement in vacuum condition again after atmosphere measure condition. After the new foming process, the device can recover to switch beween HRS and LRS again.

**The redox reaction during resistive switching**

Therefore, we infer that a redox reaction happened to the broken gap region of the $SiO_2$ substrate accounting for the memory effect. When the set voltage applied on the device, the insulating $SiO_2$ was reduced to the conductive Si, the device reach to ON state from OFF state, while the reset voltage cause the reverse process. The electrical measurements were carried out in vacuum, nitrogen and air conditions, respectively. The set process only occurs in vacuum or nitrogen but cannot be realize in air, while reset process can happen in all the conditions, shown in Figure S3 (a) and (b), indicating the reduction cannot happen in an oxygen environment, which support the redox model. The device was measured in vacuum condition again after air measurement condition. The device was reach very high resistance state due to more $SiO_x$ formation in the broken gap region in oxygen environment, then, need a higher voltage to reduce $SiO_x \rightarrow Si$, defined as new forming process. After the new forming process, devices can switch between HRS and LRS again, seeing figure S3 (c).

**More examples for multilevel switching**

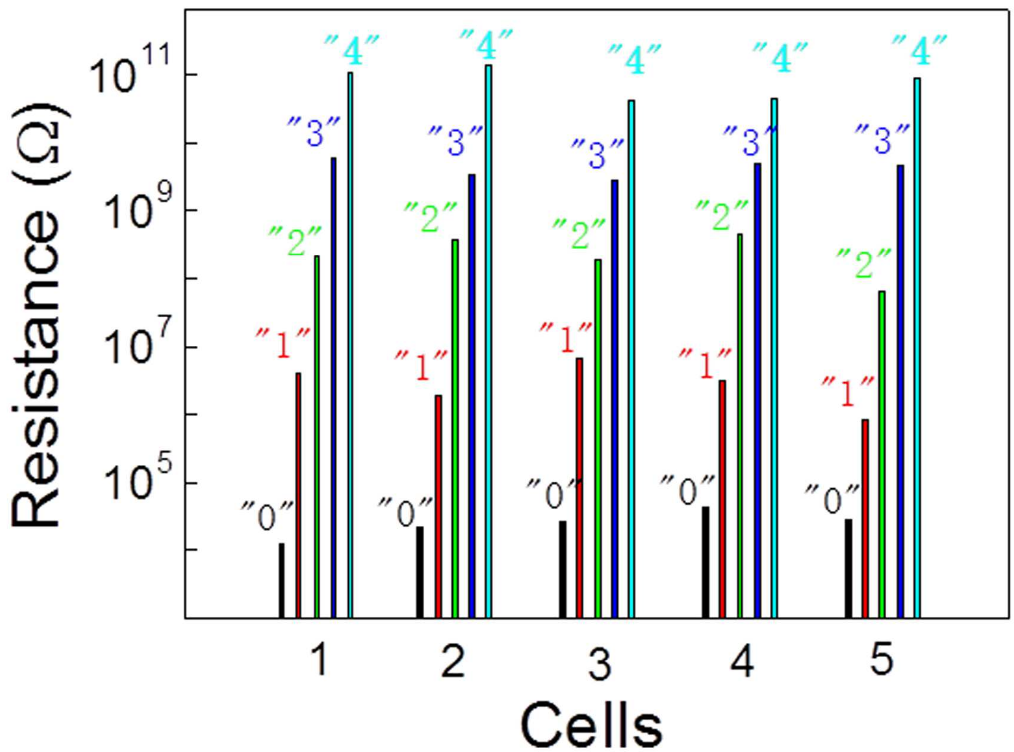


Figure S4. The multilevel switching behaviors obtained in five memory cells, demonstrating the reliable and controllable multiple-valued memory.

## References:


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