

Silicon Oxide is a Non-Innocent Surface for Molecular Electronics and Nanoelectronics Studies—Supporting Informaiton

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Material Preparations:

polySi-SiO_x-polySi: The SiO_x ($x \sim 2$) layer was grown by plasma enhanced chemical vapor deposition (PECVD) at 650 °C using tetraethyl orthosilicate (TEOS) as a precursor. The flow rates of TEOS and N₂ were 55 and 210 sccm, respectively. The growth was done at a pressure of 600 mTorr with a growth rate at ~ 2 nm per min. The polySi layers (70 nm) were grown by PECVD and implanted with boron (7×10^{15} cm⁻² at 5 KeV).

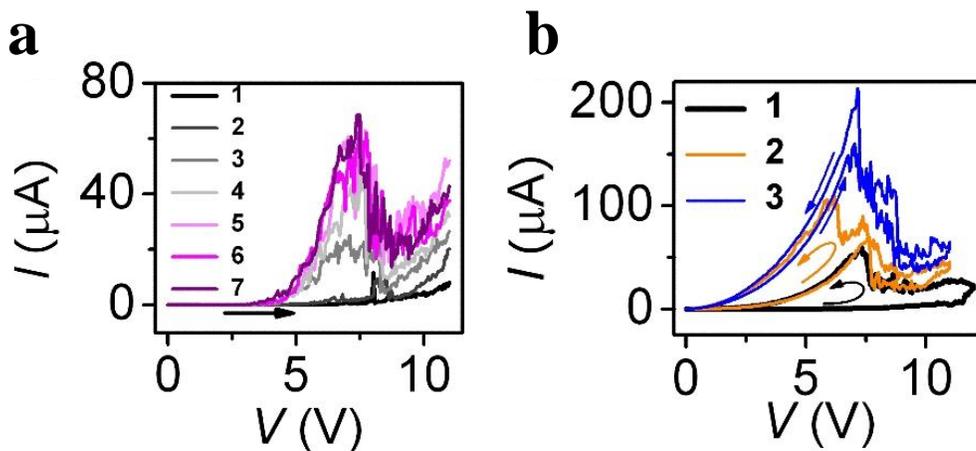


Figure S1. Electroforming processes in vertical polySi-SiO_x-polySi (70 nm-10 nm-70 nm) devices by different sweep modes. The devices have the same structure and parameters as illustrated in the main article in Fig. 1c. (a) An electroforming process by consecutive forward voltage sweeps (0 V → +11 V). Since each voltage sweep ends in the reset region, the formed device is always in an OFF state. (b) An electroforming process by consecutive loop voltage sweeps (0 V → +12 V → 0 V). Since each voltage sweep finally bypasses the set region, the formed device is always in an ON state. The arrows indicate the voltage-sweep directions and the numbers indicate the voltage-sweep orders. An electroforming process by consecutive backward voltage sweeps (e.g., +12 V → 0 V) is similar to that described in Fig. 1b in the main article.

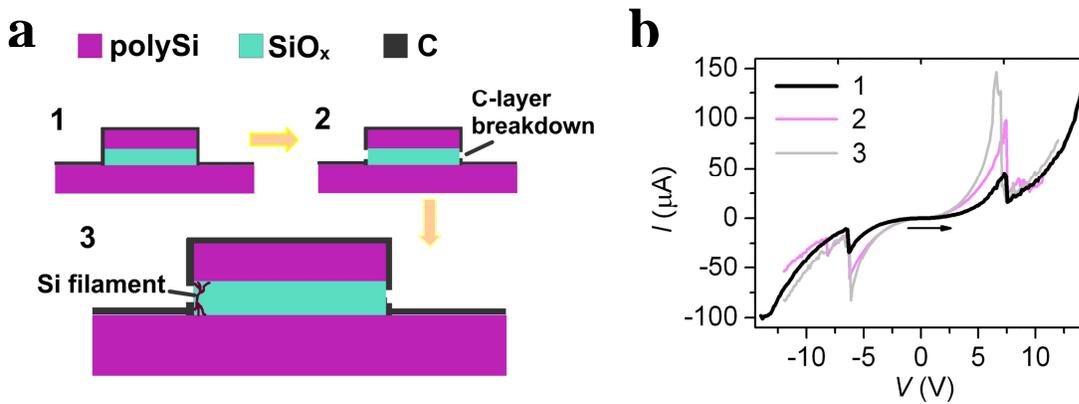


Figure S2. Resistive-switching *IV* curves in a vertical polySi-SiO_x-polySi (70 nm-10 nm-70 nm) device coated with 5 nm-thick amorphous carbon. (a). Schematics showing the C layer assists the electroforming in the SiO_x layer. 1. The initial C-coated structure. 2. Electrical breakdown in the C layer creates disruptions at the vertical SiO_x edge. 3. The disruption in the C layer enhances the local field and induces soft breakdown at the vertical SiO_x edge. An electroforming process is then initialized with the formation of Si-

NC filament. (b). The electroforming process in an actual C-coated device. The arrow indicates the voltage-sweep direction and the numbers indicate the voltage-sweep orders.

This is analogous to switching behavior observed in related systems.¹⁻³

References

1. Yao, J.; Zhong, L.; Zhang, Z.; He, T.; Jin, Z.; Wheeler, P. J.; Natelson, D.; Tour, J. M. *Small* **2009**, 5 2910-2915.
2. Li, Y.; Sinitskii, A.; Tour, J. M. *Nat. Mater.* **2008**, 7, 966-971.
3. Sinitskii, A.; Tour, J. M. *ACS Nano* **2009**, 3, 2760-2766.