Supporting information

High Current, Low Voltage Carbon Nanotube Enabled Vertical Organic Field Effect Transistors

By *Mitchell A. McCarthy, Bo Liu and Andrew G. Rinzler*

Effect of baking the nanotubes

The single wall carbon nanotubes used in these devices are charge transfer doped by their nitric acid purification. This p-dopes the nanotubes pushing their workfunction to ~ -4.9 eV. Baking the nanotubes desorbs the charge transfer dopant shifting their Fermi-level back toward their intrinsic workfunction of ~ -4.6 eV. The starting workfunction difference between the nanotubes and the organic layer dictates the initial magnitude of the Schottky barrier, establishing the baseline barrier that is modulated by the gate. Figure S1A illustrates the effect of shifting the initial nanotube Fermi level relative to the HOMO of DNTT. As shown below, the resulting increase in the initial barrier improves the performance of the devices by reducing the off current and the subthreshold slope.

To verify that baking the thin nanotube films on a hot plate in the Ar glovebox can dedope the nanotubes, films of the same nanotube density as used in the CN-VFET were transferred to 3 glass slides. The films were squares of 1 cm sides with gold electrodes touching the four corners of the films (for 4-terminal Van der Pauw measurement determination of the film sheet resistance). One of the samples was an unbaked control sample, while the other two were baked for an hour in the Ar glove box, one at 200°C and the other at 300°C. Visible-near infrared (VIS-NIR) transmission spectra were recorded by a Perkin Elmer Lambda 900 UV/VIS/NIR spectrometer. Figure S1B shows the VIS-NIR spectra for the three samples and also lists the sheet resistance of the associated film. The changes in depth of the S1 & S2 dips in the transmittance along with the changes in the sheet resistance are clear signatures of effective dedoping with increasing temperature, understood on the basis of shifts in the nanotube Fermi level.[S1]

Figure 3 of the manuscript shows the transconductance data for the CN-VFET in which the nanotube film was baked in the glovebox at 225°C for an hour prior to deposition of the DNTT.

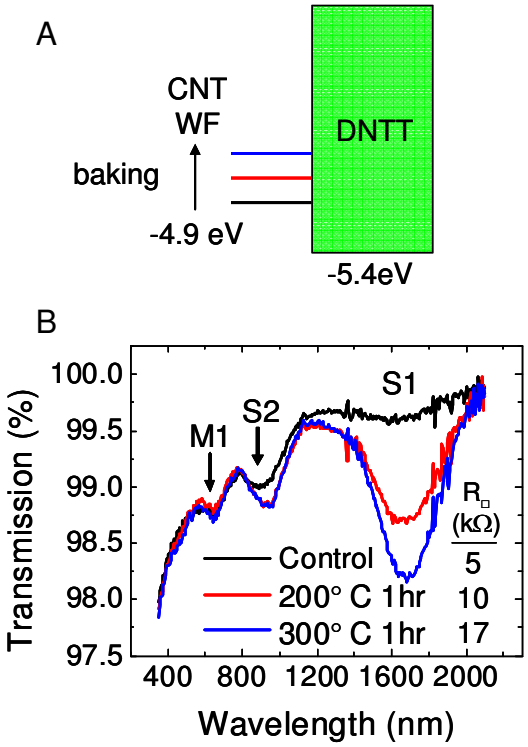

Figure S1. (A) Schematic showing the expected position of the nanotube Fermi level for the control (black line), 200°C 1hr baked (red line) and 300°C 1hr baked (blue line) films. From the transmission spectra in B) it is expected that the nanotube Fermi level moves 2-3 tenths of an eV during baking. (B) Transmission spectra for a nanotube network of the typical density used in the CN-VFET under different baking conditions.

Figure S2 compares the transfer curves for a CN-VFET that did not have such a de-doping bake with one that did. The device data in Figure S2 were from devices fabricated the same way as in the main paper except that the DNTT layer was 570 nm thick (as opposed to the 480 nm in the main paper). That the unbaked (doped nanotube) device can't be turned off at the maximum positive gate voltage is consistent with the deeper workfunction of the doped nanotubes, possessing a smaller native Schottky barrier with the DNTT. For a conventional transistor the larger subthreshold slope for the unbaked device would be indicative of a greater density of interface traps at the nanotube/BCB interface in that device.[S2] However, the interpretation of the subthreshold slope in these devices remains under investigation.

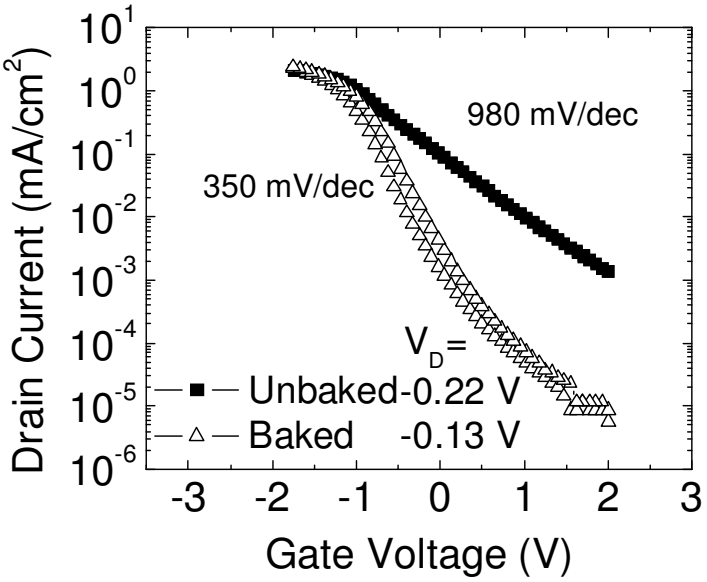

Figure S2. Transfer curves of CN-VFETs that had a baked nanotube source electrode (prior to DNTT deposition) compared to an unbaked nanotube source electrode device. In the ON-state, when V_G = -1.75 V, voltage is applied to both devices until I_D = 2.3 mA/cm^2. For the unbaked device this occurs at V_D =-0.22 V and for the baked device at V_D = -0.13 V. As a result of baking the nanotube film, the SS slope decreases significantly and the on/off ratio increases by two orders of magnitude.

Current density calculation for lateral channel TFTs

To compare TFTs and VFETs in terms of the current output per unit device area, a sensible figure of merit is defined. A TFT with an interdigitated source-drain electrode configuration is assumed. The width of each source and drain electrode is taken to be the same as the channel length L from the published work, to maintain the minimum feature size (the channel length in all the TFT devices). Using the maximum on-drain current, I_D, per unit channel width W, and channel length L, into $J_{Eff} = I_D/(2*W*L)$, an effective areal TFT current density is obtained. Figure S3 shows a schematic of the interdigitated configuration where the dotted line encloses the effective area given by this calculation. Calculation of the areal current density for the CN-VFET does not include the area of the source contact, however, the area calculated for

the lateral TFT does not include area of the "bus bars" feeding the fingers so the comparison remains fair.

$$J_{Eff.} = \frac{I_D}{A} = \frac{I_D}{2*W*L}$$

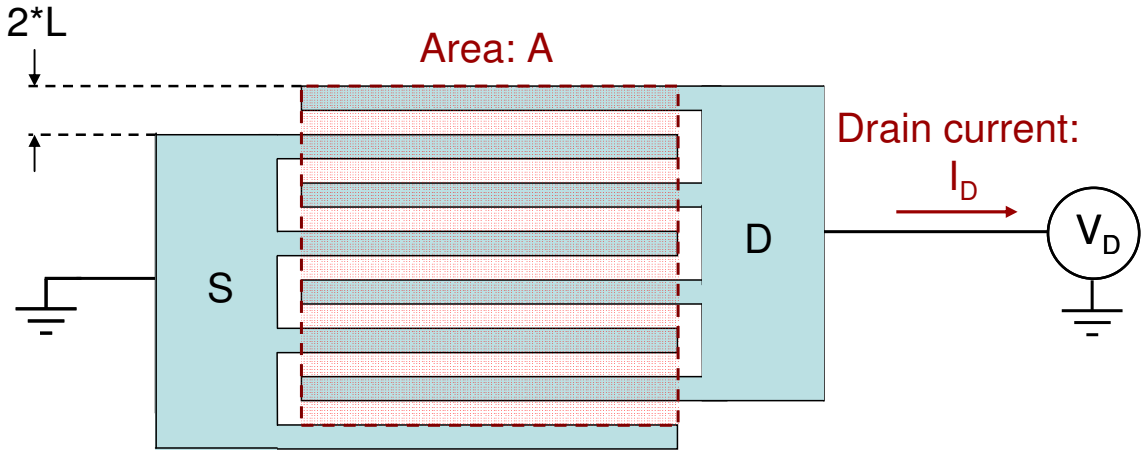

Figure S3. Interdigitated source-drain electrode configuration used to calculate the figure-of-merit J_{Eff} to compare current outputs of TFTs and VFETs.

Optical microphotographs of the CN-VFET devices

Figure S4A shows an optical image of the entire substrate of the CN-VFET devices. Outlined in red dotted lines are the CNT source electrodes which are too dilute to be visible in the image. Au coated needle probes are used to make contact to the source and gate electrodes and an Au wire is used to make contact to the drain pixel as shown in Figure S4B.

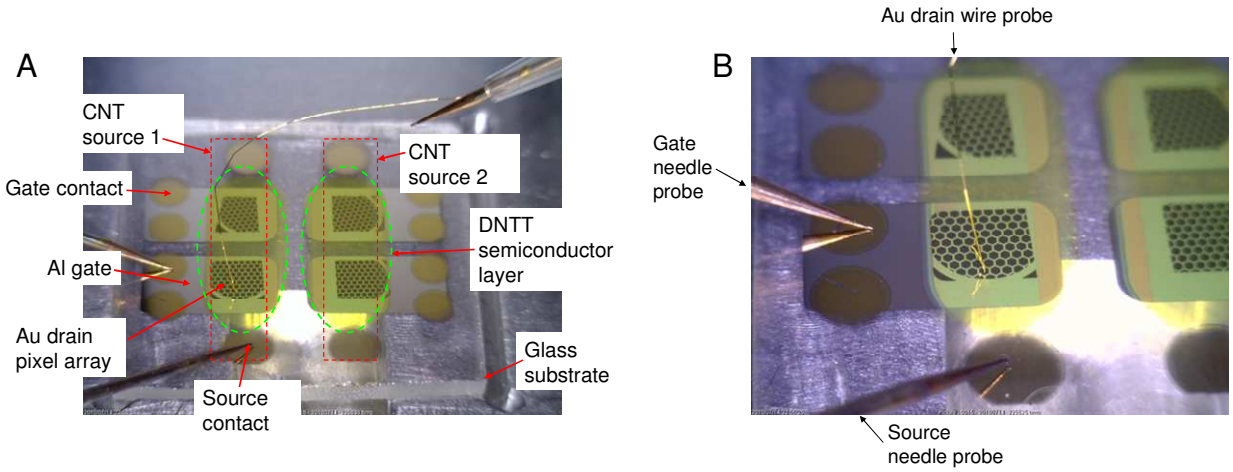

Figure S4. (A) Labeled full-view image of the 0.6" by 0.6" square glass substrate and numerous distinct DNTT CN-VFETs, defined by each hexagonal drain electrode. (B) Zoomed-in image showing the source, and gate contact probes as well as the drain contact to one CN-VFET device. Images recorded in a microprobe station within the argon glovebox.

References

S1. Z. C. Wu, Z. H. Chen, X. Du, J. M. Logan, J. Sippel, M. Nikolou, K. Kamaras, J. R. Reynolds, D. B. Tanner, A. F. Hebard, A. G. Rinzler, Science 2004, 305, 1273.

S2. Chang, M. R.; Lee, P. T.; McAlister, S. P.; Chin, A. Ieee Electron Device Letters 2008, 29, (3), 215-217.