

Methods

Two structures were fabricated in this work, both of which started with the same basic structure depicted in Figure 1a, with the two structures having different masked areas and consequently different regions on which the nanowires could nucleate. The first structure can be seen in cross section and plan view SEM in Figure 2. Its fabrication is schematically depicted in Figure 1 (path 1 from Figure 1a-1c). The second structure is the MOSFET structure shown in the TEM images in Figure 3; its fabrication is schematically depicted along path 2 in Figure 1.

Both structures discussed in this letter started with a (100) SOI wafer from SOITEC with a 100 nm, (100)-oriented Si layer on top of a 200 nm buried-oxide layer (BOX). Both the top Si layer and the handle wafer were lightly doped with boron to a resistivity of $\sim 18 \text{ Ohm}\cdot\text{cm}$. The top Si layer was implanted with phosphorus at 55 keV to a dose of $4 \times 10^{14} / \text{cm}^2$ to ensure that it was heavily n-type. The wafer was then RCA cleaned and placed in a furnace with a N_2 ambient at 900°C for 30 min to activate the dopant atoms and remove implant damage. The wafer was then dipped in 10:1:: NH_4F :HF (BOE) just prior to depositing a 70 nm Si_3N_4 film at 780°C . The nitride film was patterned with trenches parallel to the $\langle 110 \rangle$ direction and used as a hard mask to etch the underlying Si with KOH at 80°C to reveal the angled (111)-type Si sidewalls schematically shown in Figure 1a.

For the first structure (path 1 in Figure 1 and SEM of Figure 2), about 80 nm of BOX was etched using BOE to undercut and uncover a small portion of the bottom of the Si layer.

It was then exposed to 3 parts of unconjugated, Au colloid supplied by Ted Pella containing 40 nm diameter Au nanoparticles, and 2 parts of 5% HF for 30 s to deposit Au nanoparticles on the Si surface to act as a catalyst for the Si nanowire growth. The sample was annealed at 400 °C in a H₂ ambient—above the 363 °C Au-Si eutectic temperature—so that those Au nano particles in contact with Si alloyed with the Si. Au nanoparticles on the oxide and nitride surfaces did not alloy and were then removed by dipping the sample in BOE for 7 s and H₃PO₄ (at 155 °C) for 2.5 min to etch some of the oxide and nitride, respectively. This etching resulted in Au nanoparticles remaining only on exposed Si surfaces; namely, the KOH-etched, angled surface and the undercut Si surface, as shown schematically on the left and right sides of Figure 1b, respectively. Si nanowires were grown for 37.4 s at 680 °C under the following conditions: 3 slm H₂, 30 sccm SiH₄, 30 sccm HCl, at 95 torr (Figure 1c).

Fabrication of the second structure followed path 2 shown schematically in Figure 1. After the structure in Figure 1a was fabricated, a second layer of nitride (70 nm) was deposited and was used as part of a self-aligned process to leave nitride on the angled Si edges after a second reactive-ion etch (RIE) (Figure 1d). As was done for structure 1, the sample was dipped in BOE to etch about 80 nm of BOX and to slightly undercut the n⁺-Si. The sample was patterned again and etched using RIE to remove some of the nitride on top of the source and drain to facilitate later Al source-drain contact formation. The nitride on the back of the wafer was also removed via RIE to allow later backside electrical contact. The wafer was dipped in BOE for 7 s, rinsed and dried. It was then exposed to unconjugated Au colloid from Ted Pella containing 100 nm diameter Au

nanoparticles and 5% HF in the ratio of 3:2 for 30 s, rinsed and dried. The 100 nm Au colloid had a lower nano particle density compared to the 40 nm Au colloid ($5.6 \times 10^9/\text{mL}$ for 100 nm colloid compared to $9 \times 10^{10}/\text{mL}$ for 40 nm colloid), consequently, the density of the deposited nanoparticles and the subsequently grown NWs were also reduced. After catalyst deposition, the sample was annealed in a H_2 ambient at 400°C to alloy the Si with the Au. The sample was then dipped in BOE and H_3PO_4 as discussed above to remove stray Au nanoparticles (Figure 1e). Nanowires were grown for 31 s at 680°C under the following conditions: 3 slm H_2 , 30 sccm SiH_4 , and 30 sccm HCl at 95 torr. After the nanowires were grown, the sample was soaked in Aqua Regia for 15 min to remove the gold nanoparticles. The gate oxide was next grown at 800°C for 20 minutes in an O_2 ambient. The sample was then patterned, and 200 nm of Al was electron-beam evaporated to form contacts to the source and drain (Figure 1f). The sample was annealed at 400°C under 3.9% H_2 forming gas for 30 min to remove evaporation damage and passivate interface states. Finally the device was patterned, and a top Ti gate, 170 nm thick, was electron-beam evaporated onto the device, after which the sample was again annealed at 400°C in forming gas for 30 min to remove evaporation damage (Figure 1g and 1h).