**Supplementary Section**

Detailed explanation of the electrical properties of NWs.

The electrical properties of a different GST nanowire device (different from the main text) are shown in Figures Supplementary 1 (a) and (b). The nanowire device was fabricated by using the FIB technique using Pt as contact metal.

![Figure 1](image1.png)

FIG. Supplementary 1. Electrical behavior of Ge$_2$Sb$_2$Te$_5$ NW device different from the one shown in the main text. (a) I-V characteristics of the crystalline Ge$_2$Sb$_2$Te$_5$ NW device (circles). The I-V characteristics of the NW after applying a current pulse (0.6 mA, 100 ns) that leads to amorphization is shown as squares. (b) R-I characteristics of the Ge$_2$Sb$_2$Te$_5$ NW device as a function of applied current pulses with varying amplitudes; starting from the crystalline SET state (squares) and then from the amorphous RESET state (circles).

The as-synthesized GST NW memory device initially displayed ohmic behavior (red circles) with a low resistance of ~7 kΩ (Fig. Supplementary 1(a)), which is attributed to their original crystalline “SET” state. To probe the phase transition behavior of the NW, short 100 ns electrical pulses with varying current amplitudes were applied to the device followed by measurements of resistance values at a bias of 0.2 V (Fig. Supplementary 1(b), squares). Short current pulses produce an amorphous state due to the rapid heating and quenching of the material. For current pulses up to ~0.45 mA, very small changes were observed in the resistance values, however higher current pulses induced crystalline to amorphous phase transition leading to increased resistance (RESET state), until saturation value of ~3.0 MΩ is reached. The I-V behavior of the RESET state with resistance of ~3.0 MΩ is shown in Fig. Supplementary 1(a), (squares). The device shows extremely high resistance (3 MΩ) until a threshold voltage ($V_{th}$) of ~1.1 V, above which due to the large heat generated in the NW causes amorphous to crystalline phase transition, leading to high currents. At higher applied voltages (>1.5 V), highly crystalline NW (SET state) is achieved and the I-V curve coincides fully with that obtained from the as-synthesized GST NW. The region where the two I-V curves coincide is known as dynamic conduction state and is used for the “programming” of the
devices between SET and RESET states.

To study the current pulse amplitude dependence of the transition from amorphous to crystalline state, the GST NW device was switched back to amorphous state by applying a 100 ns pulse with a current amplitude of 0.6 mA. Longer pulses (300 ns) with varying current amplitudes were applied and the resistance of the NW was measured at each step (Supplementary Fig. 1(b), circles). Long current pulses initiate amorphous to crystalline phase transformation by inducing nucleation and growth of crystallites in the material. The resistance of the NW dropped dramatically for current amplitudes greater than 0.28 mA, which is due to amorphous to crystalline transition. A stable lower resistance state (SET) was achieved for current pulses up to ~ 0.4 mA, whereas higher current pulses prepared the system back to the amorphous (RESET) state. The programming curves given in Fig. Supplementary 2(b) clearly separate the different regions associated with SET, RESET and Read (regions which are not affected by the current) states. Therefore, our results clearly demonstrate the fully reversible phase transition behavior in GST NWs.

Overall, 8 NW devices were fabricated by using the FIB technique using Pt as contact metal. Of the 8 devices, 6 NWs were observed to be electrically active, while the other two did not show any electrical activity, possibly due to poor contacts. All the 6 devices showed reversible phase-transition switching behavior as detailed in the main section of the paper. The electrode spacing for all devices was fixed at 2 µm. The SET state resistance varied from 1.7x10^4 Ω to 2.2x10^4 Ω, whereas the RESET state resistances varied from 2.4x10^6 Ω to 3.0x10^6 Ω. The RESET currents varied from 0.43 mA to 0.50 mA, while the SET currents varied from 0.25mA to 0.33 mA.

A complete RESET state is obtained with a current pulse of 0.6 mA, i.e., on applying current pulses of higher amplitude, very little increase in resistance of RESET states are obtained. However, for any practical device, it is not necessary to switch between complete RESET and SET states, as it leads to unnecessary high power consumption and longer pulse write/erase time. The most important figure of merit in memory switching devices is the “sensing margin”, i.e., the ratio of RESET to SET resistance. From Fig. 2(b) of the main text, it can be seen that upon application of current pulses of amplitude more than 0.43 mA, significant changes in resistance of the NW takes place and hence a large sensing margin can be obtained, which is sufficient to “sense” the device states as between RESET and SET states. In case of Fig.2b (main text), in order to obtain the critical value of the RESET writing current displaying the difference of reset and set resistance, R-I curve was evaluated. In summary, the nanowire cell showed large resistance change for memory sensing margin (data “1” and data “0”) above 0.43mA

Our nanowire memory devices are operated under voltage control for read and write (SET/RESET) process. In general, phase transition random accessing memory (PRAM) devices fabricated at various companies are operated by voltage (operation or supply voltage) control at the peripheral circuit level. Operation voltage in circuit is controlled in order to apply a certain current amplitude for writing/erasing. Therefore, the
nanowire memory cell can be also operated under current control, which would require fabricating a complex circuit to deliver the required current pulses to the device.

**RESET and SET Reversibility of the NW device after multiple cycling test.**

The reversibility of the GST NW memory switching device was evaluated by applying a pulse cycle as shown in the inset of Fig. Supplementary 2. A RESET pulse of 0.5 mA amplitude and 100 ns duration was applied and the resistance was measured at an applied bias of 0.2 V. Then a SET pulse (0.3 mA, 300 ns) was applied followed by measurement of the resistance (at 0.2 V). Thirty such pulse sequences were applied and it was observed that the device recovered the resistance values in both SET and RESET states, thereby showing complete reversibility.

![Graph showing resistance values over number of cycles](image)

**FIG. Supplementary 2.** Cycling test of the Ge$_2$Sb$_2$Te$_5$ NW device by applying RESET and SET pulse cycles as shown in the inset.

**Power consumption of the Device.**

The power needed to achieve RESET and SET states can be calculated as follows:

- \( R_{dy} \) (resistance at dynamic conducting state) \( \sim 7k\Omega \), obtained from the I-V curves.
- \( V_{th} \) (threshold switching voltage) \( \sim 1.1 \) V or \( I_{th} \) (threshold switching current) \( \sim 0.16 \) mA
- \( I_{reset} \) (writing current for RESET state)\( \sim 0.43 \)mA,
- \( I_{set} \) (writing current for SET state) \( \sim 0.25 \)mA

Since the \( I_{reset} \) and \( I_{set} \) values are higher than \( I_{th} \), we have to consider resistance value of dynamic state for determining the power consumption.

\[
P_{reset} \text{(power consumption for RESET state)} = 0.43 \times 0.43 \times 10^{-6} \times 7 \times 10^3 = 1.294 \text{mW}
\]
\[
P_{set} \text{(power consumption for SET state)} = 0.25 \times 0.25 \times 10^{-6} \times 7 \times 10^3 = 0.44 \text{mW}
\]

These values can be truly considered “extremely low power consumption” even in comparison to state-of-the-art devices fabricated commercially (~6.0mW and ~3.6mW values for RESET and SET, Reference: *VLSI Tech. Dig.*, 2004, 20.).