Supporting Information for: Fundamental Limits on the Subthreshold Slope in Schottky Source/Drain Black Phosphorus Field-Effect Transistors

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Device Fabrication Process

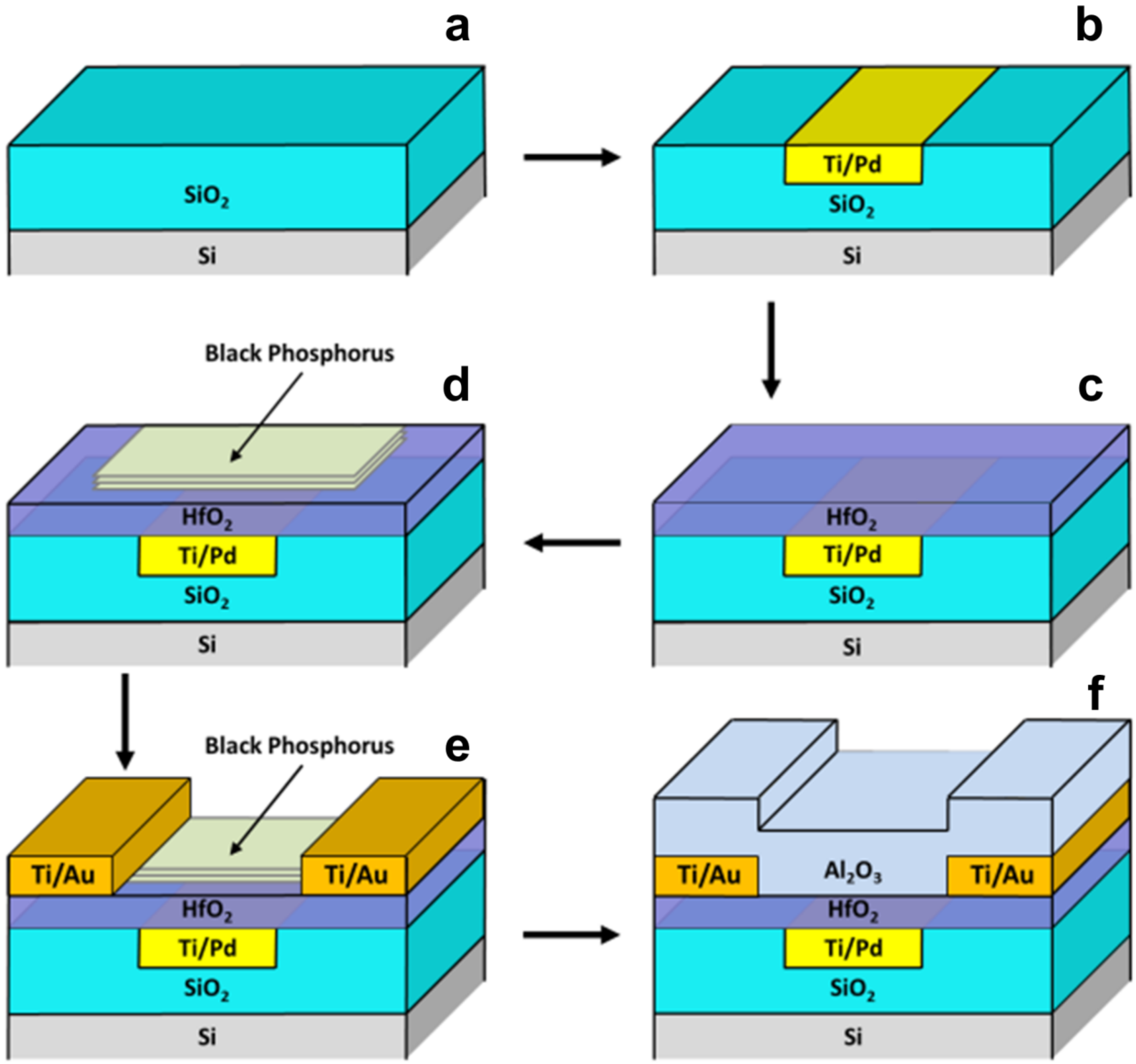

Figure S1. Fabrication sequence for BP MOSFETs. (a) Si/SiO_2 starting substrate, (b) local back gate formation, (c) ALD HfO_2 deposition, (d) black phosphorus alignment and transfer, (e) source and drain contact formation, (f) ALD Al_2O_3 passivation layer deposition.

Optical Micrographs of Additional Devices

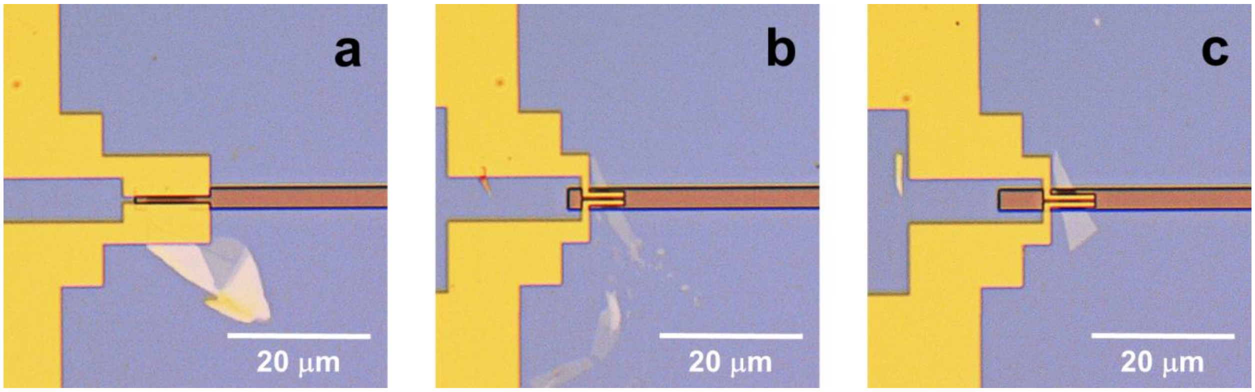

Figure S2. Optical micrographs of several completed BP MOSFETs. (a) Device #2 with BP thickness (in the active device region), t_{BP} of 4.3 nm. The device width, W_g was 7.15 μm and the source-to-drain spacing, which defined the effective gate length, L_{eff} was 1.0 μm. (b) Device #3 with t_{BP} = 4.5 nm, W_g = 2.00 μm and L_{eff} = 0.4 μm, and (c) Device #7 with t_{BP} = 8.1 nm, W_g = 3.16 μm and L_{eff} = 0.30 μm.

Black Phosphorus Raman and Reflectance Characterization

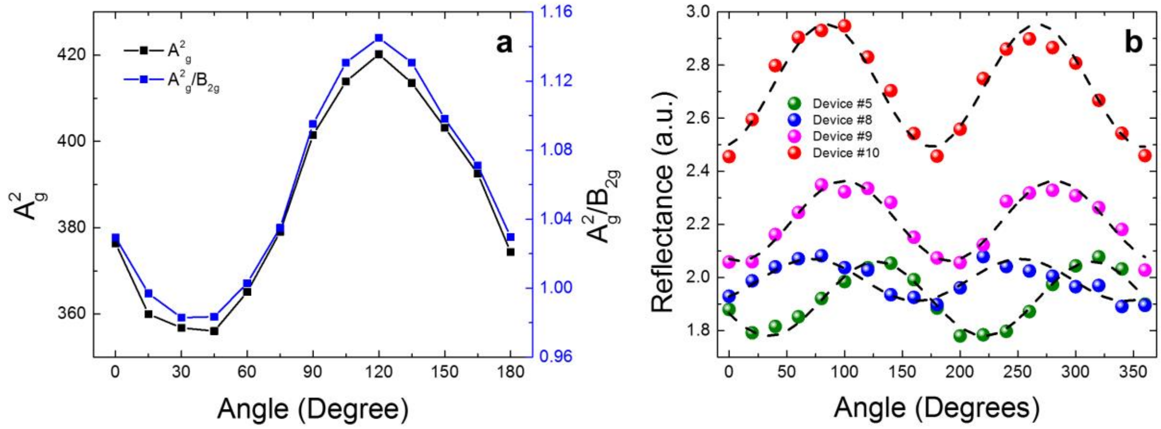

Figure S3. (a) Angular dependence of the Raman $A^2{}_g$ mode (left axis) and $A^2{}_g/B_{2g}$ (right axis) for a typical BP flake. The peak intensity is the direction that the laser polarization is along the armchair (low mass) direction. (b) Reflectance intensity as a function of rotational angle for devices #5, 8, 9, and 10. The maximum peak intensity indicates the zigzag direction (high mass). Dashed lines shows the sinusoidal fit of the reflectance data.

Double Sweep Transfer Characteristics

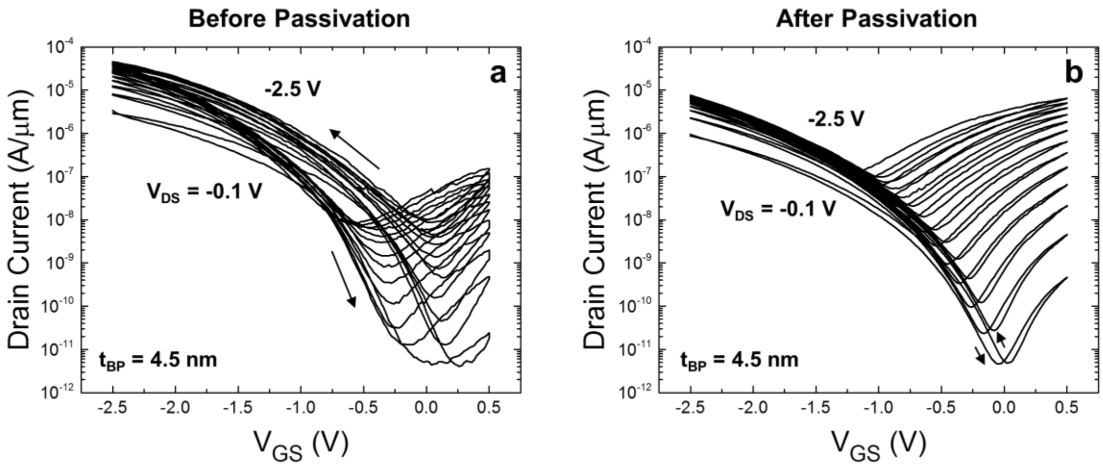

Figure S4. Double sweep transfer characteristic of device #3 (a) before and (b) after passivation for values of $V_{DS} = -0.1$ to -2.5 V in -0.2 V steps. Possible causes for the hysteresis include charge trapping in the HfO_2 gate dielectric, moisture trapped underneath the BP, and/or surface oxide layers on top of the BP. The hysteresis was greatly reduced after passivation, which we attribute to moisture desorption during the passivation layer deposition step at 200°C.

Output and Transfer Characteristics

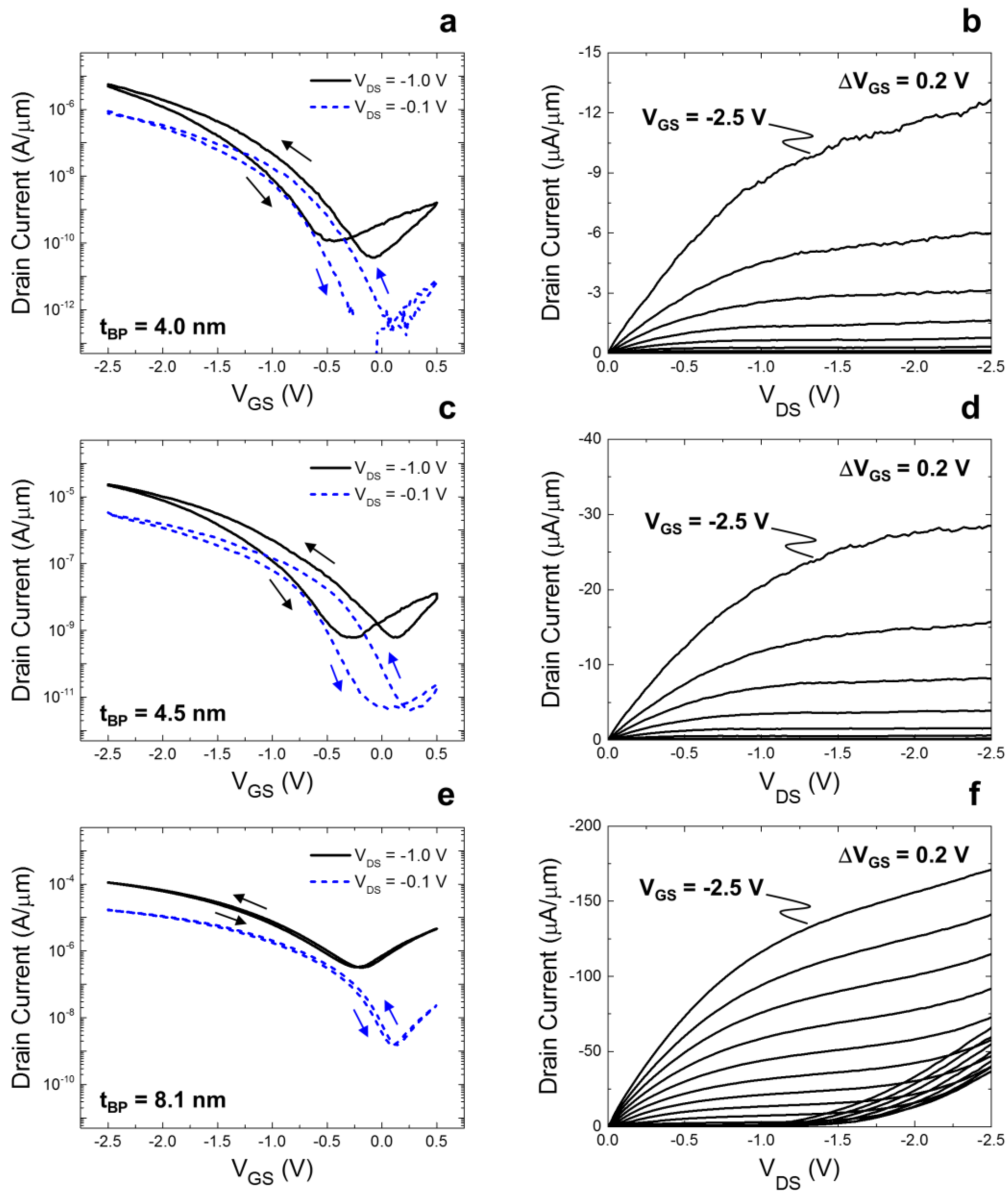

Figure S5. Room-temperature current-voltage characteristics of (a)-(b) device #1 (t_{BP} = 4.0 nm) before passivation, (c)-(d) device #3 (t_{BP} = 4.5 nm) before passivation, and (e)-(f) device #7 (t_{BP} = 8.1 nm), after passivation. (a), (c) and (e) are plots of drain current, I_D, *vs.* gate-to-source voltage, V_{GS}, for both forward and reverse sweep directions at drain-to-source voltage, V_{DS} = –0.1 V (blue) and -1.0 V (black). (b), (d) and (f) show plots of I_D *vs.* V_{DS} for the same devices where the top curves are at V_{GS} = –2.5 V and the gate voltage step, ΔV_{GS} = +0.2 V.

Black Phosphorus Stability Analysis

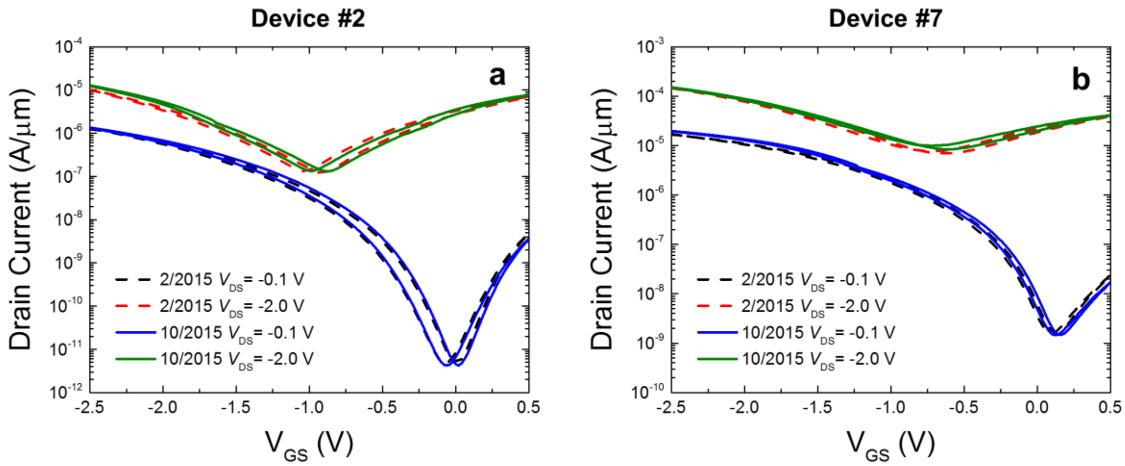

Figure S6. Comparison between the initial I_D *vs.* V_{GS} characteristic of (a) device #2 and (b) device #7 immediately after passivation (in 2/2015) and the characteristics after ~ 8 months (in 10/2015). The devices were stored in a nitrogen purged dry box, but were exposed to air occasionally for characterization periodically during this time. Before the measurements shown on 10/2015, the devices were first baked at 200 °C for 30 minutes. As shown in the figure, the threshold voltage and basic characteristics were completely retained, both at low and high values of V_{DS}. These results demonstrate the potential for long-term stability in black phosphorus MOSFETs passivated with Al_2O_3.