Supporting Information

Enabling Gate Dielectric Design for All-Solution Processed, High-Performance, Flexible Organic Thin-Film Transistors

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1. Instrumentation

Advancing water contact angle was measured on a DAT 1100-Fibro System using deionized water. Capacitance was measured with a BK Precision 820 capacitance meter (Dynascan Corporation). Thickness of thin film was measured with a Dektak 6M Stylus Profiler. OTFTs were characterized using Keithley SCS-4200 Characterization System under ambient conditions.

2. Synthesis of poly(methyl silsesquioxane).

Poly(methyl silsesquioxane) was prepared using methyltrimethoxysilane as precursor as follows: A mixture of 0.88 grams of 0.1 wt% aq. hydrochloric acid solution and 5.13 grams of tetrahydrofuran was added dropwise over a period of 30 minutes to a rigorously stirred mixture of 4.08 grams of methyltrimethoxysilane and 9.24 grams of methylisobutylketone in a 3-necked flask cooled with an ice bath under a dry atmosphere.

The resulting mixture was allowed to warm to room temperature and then stirred at 60° C for 24 hours before subsequent use as the modification agent.

3. Deposition of Gate electrode.

Polyester substrate was first subject to heating at 160 °C for 10 min, cooled to room temperature and cleaned with isopropanol before use. A 7 wt% dispersion of butanethiol-stabilized gold nanoparticles [Ref. Wu, Y.; Li, Y.; Ong, B.S.; Liu, P.; Gardner, S.; Chiang, B. *Adv. Mater*. **2005**, *17*, 184-187] in cyclohexane was filtered through 0.2 μm syringe filter, and then spin coated on the polyester substrate at 1000 rpm for 30 s. The coated gold nanoparticle layer was air dried and annealed in a vacuum oven at 150 °C for 30 min, resulting in a 90 nm-thick conductive gold layer on the polyester substrate. The surface of the gold layer was cleaned with air plasma for 30 seconds before subsequent deposition of gate dielectric.

4. Preparation of dual-layer gate dielectric layer.

A 13 wt% of poly(vinyl phenol-co-methyl methacrylate) (PVP-co-PMMA) (obtained from Aldrich, 51 mol % vinyl phenol) in DMF solution was filtered through a 0.2 μm syringe filter, and then deposited by spin coating on top of the above gold layer on the polyester substrate. The resultant 420-nm PVP-co-PMMA thin film was dried at 60 °C for 30 min and then annealed at 140 °C for 10 min. After cooling to room temperature, the PVP film was irradiated with an UV light (λ = 254 nm) for 20 min, and then immersed in n-butanol at 60 °C to remove the unreacted polymer, giving a 380-nm crosslinked PVP-co-PMMA film after drying. Thereafter, a thin layer of poly(methyl silsesquioxane) (~ 50 nm) was spin coated on top of the PVP-co-PMMA layer and then

cured by heating at 160 °C for 1 hour on a hot plate. The capacitance of the resulting dual-layer dielectric was measured to be 9.0 nF/cm^2 with a BK Precision 820 capacitance meter (Dynascan Corporation) at room temperature. The dielectric constant of the dielectric layer was calculated to be 4.0.

5. Fabrication of source/drain electrodes and deposition of semiconductor.

A 7 wt% dispersion of gold nanoparticles in cyclohexane was deposited on the dielectric surface via a mask-assisted microcontact printing as follows. A stainless steel mask (thickness ~ 13 μm) with an array of source/drain electrode feature apertures was placed on top of the dual-layer dielectric. A PDMS rubber sheet spin coated with a thin film of gold nanoparticles was laid on top of the mask. A gentle pressure was applied to the PDMS sheet to force the gold nanoparticle film to make contact with the dielectric surface through the apertures of the mask. After about 2 min, both the mask and the PDMS sheet were lifted, leaving the gold nanoparticle electrode features on the dielectric surface. The printed features of gold nanoparticles were annealed in a vacuum oven at 150 °C for 30 min, resulting in the formation of gold source/drain electrode pairs with channel lengths of 90 to 400 μm and channel widths of 1000 to 5000 μm. Finally, a 30-nm thick of PQT-12 semiconductor layer was deposited by spin coating a dispersion of PQT-12 nanoparticles in dichlorobenzene, and annealed at 140 °C for 20 min. [Ref. Ong, B. S.; Wu, Y.; Liu, P.; Gardner, S. *Adv. Mater*. **2005**, *17*, 1141-1144].

6. Characterization of OTFTs.

The OTFTs were characterized in air using a Keithley 4200 Semiconductor Characterization System. The mobility in the linear and saturated regimes was extracted from the following equations:

Linear regime ($V_D << V_G$): $I_D = V_D C_i \mu (V_G-V_T) W/L$

Saturated regime ($V_D > V_G$): $I_D = C_i \mu (W/2L) (V_G-V_T)^2$

where I_D is the drain current, C_i is the capacitance per unit area of the gate dielectric layer, and V_G and V_T are respectively the gate voltage and threshold voltage. V_T of the device was determined from the relationship between the square root of I_D at the saturated regime and V_G of the device by extrapolating the measured data to $I_D = 0$.

Figure S1 shows the I-V characteristics for both forward (positive to negative) and reverse (negative to positive) scans at a source-drain voltage of -40V. The device exhibited only small hysteresis effect.

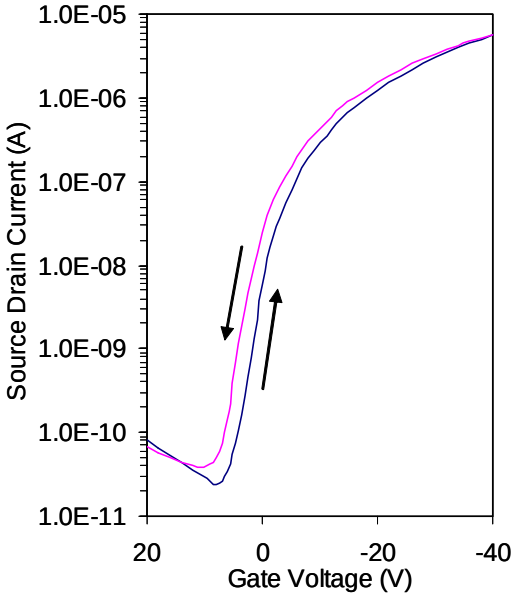

Figure S1. Forward and reverse scans of I-V characteristics at a source-drain voltage of -40 V for a typical OTFT with the dual-layer gate dielectric.