Supporting Information for

A Noninvasive Method for Nanoscale Electrostatic Gating of Pristine Materials

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Methods

The flip-chip assembly consists of a gate-chip and a material chip, an 8×8 mm quartz piece used as base and additional quartz supports to hold the gate-chip in place. The material chip is first glued onto the quartz base using S1805 photoresist. Then two quartz supports with the same thickness as the material chip are glued on either side of the material chip on the 8×8 mm piece. Afterwards, droplets of photoresist are placed on these quartz supports and the gate-chip is positioned over the material chip and quartz supports in a mask aligner. After alignment, a small force is applied onto the gate-chip to fix the setup while the glue dries (for ~12 h). The flip-chip assembly can then be safely transferred out of the cleanroom without dust entering between the chips. The assembly is glued directly on the cold finger of the cryostat and all contacts are connected to a PCB board through a combination of wire bonding, indium soldering and use of silver paint. Next, copper clamps are placed onto the gate-chip. Springs attached to the cold finger can adjust the force exerted by the copper clamps. The forces and positions of the clamps are fine-tuned such that a uniform dark blue color is observed suggesting close and uniform spacing between the chips. This color originates from the interference between the reflected light from the surface of the material chip and the reflected light from the bottom surface of the gate-chip. A dark blue color suggests a separation of ~100 nm between the gate and the surface of the material chip, and a uniform color signals uniform spacing. Figure 1c shows the flip-chip assembly mounted on the cold finger including the copper springs. The whole setup is free from magnetic parts and fits in a standard 2 inch magnet bore.
Figure S1: Depletion voltage for the continuous gate that spans the width of the 2DEG in assembly A in the main text. (a) Four-terminal conductance as a function of the voltage on the continuous gate (indicated by red in the false-colored SEM image in a). The gate has a width of 8.3 µm, much wider than the average gate-heterostructure separation of ~100 nm. Therefore, the parallel plate capacitor model (b) is justified for estimating the vacuum gap between the two chips. At a voltage of $V_{\text{continuous}} = -2.2$ V the conductance drops to zero, indicating that all electrons underneath the gate are depleted. The gate-2DEG coupling can be described by the capacitor network depicted in b. $C_{\text{GaAs}}$ is the capacitance per unit area between the 2DEG and the surface of the GaAs. The capacitance between the gate and the surface of GaAs is $C_{\text{vac}} = \varepsilon_0 \varepsilon_r / d$ per unit area. The total capacitance between the 2DEG and the gate is $C_t = 1/(1/C_{\text{vac}} + 1/C_{\text{GaAs}})$.

Using $en = C_t V_{\text{continuous}}$ and $V_{\text{continuous}} = -2.2$ V, a density of $n = 1.35 \times 10^{11}$ cm$^{-2}$ (obtained from Hall measurements), a depth of the 2DEG of 100 nm, we estimate that $d = 84$ nm.

The vibration amplitude between the two chips is estimated using the blur at the zero-bias crossings of the Coulomb diamonds. From Fig. 3a in the main text we estimate a 20% blur (0.15 mV in $V_8$). A change in $d$ affects the island potential through all six gates ($V_{8,11} = -2.5$ V, $V_{9,12} = -3.27$ V and $V_{7,10} = -3.32$ V). The capacitance of the island is $C_i = C_0 + C_g$, where the $C_0$ is the self-capacitance and $C_g$ the capacitance to the gates, which is predominantly the capacitance over the vacuum gap (because the dielectric constant of GaAs is 12x larger than vacuum). The plunger gate capacitance is $\sim C_g/3$ (4 µm over 13 µm) by comparing the lengths of the gates. Using the capacitor model in b) we relate the change in capacitance to a change in separation $\Delta C_g / C_g = \Delta d / d$. The charge induced by change of the plunger gate $\Delta V_g$, $\Delta Q = C_g / 3 \cdot \Delta V_g$, should equal the charge induced by a change in chip separation, $\Delta Q = \Delta C \cdot V_g = C_g (\Delta d / d) \cdot V_g$. Thus an upper bound on the vibration amplitude is given by $\Delta d = d \Delta V_g / 3V_g = 1.5$ pm, using $V_g = -2.8$ V, $d = 84$ nm and $\Delta V_g = 0.15$ mV.
**Figure S2: Parallel plate capacitor.** (a) Tilted scanning electron micrograph of a quartz chip with a metallic square of 240 µm x 240 µm. The posts are ~100 nm higher than the metallic square and the surrounding quartz is etched 4 µm deep. The scale bar represents 100 µm. This quartz chip is flipped over and put onto the other quartz chip with the same metallic square but with neither posts nor etching. (b, c) Optical images of the two chips during and after alignment. (d) The full flip-chip assembly consisting of a parallel plate capacitor.

The two metallic squares act as a parallel plate capacitor from which the average distance is extracted by measuring the capacitance. The assembly is placed inside a nano-manipulator that is used to apply a variable force on the top of the assembly. Capacitance is measured using a lock-in amplifier. A sinusoidal voltage of 1 V$_{rms}$ is applied between the two plates at a frequency of 7.9 kHz. A measured current of 200 nA (Y-component) translates into 4 pF between the two capacitor plates resulting in an average separation of 120 nm. Precautions are taken to minimize the shunt capacitance of the wires to <0.2 pF.

**Figure S3: Characterization of the right QPC for assembly A in the main text.** (a) Conductance as a function of the voltage on the right QPC (gates 9 and 12) in both sweeping directions. The electrons in the 2DEG underneath the gates are depleted at -2.2 V and pinch-off of the QPC occurs at -3.3 V. (b) Quantized conductance steps near pinch-off, similar to the left QPC shown in Fig. 2c and d in the main text.
**Figure S4: Coulomb peaks as a function of time for assembly A in the main text.** By scanning the plunger gate voltage \((V_8 = -2.5 \text{ V} + \Delta V_8)\) over a 3 mV range, five Coulomb peaks of a quantum dot are probed at a voltage bias of \(V_b = 10 \text{ µV}\). This trace is repeated 50 times during ~90 minutes. A slow drift in the Coulomb peak positions is observed. After 90 minutes, one extra electron has entered the quantum dot. Such drift may result from relaxation in the 2DEG and/or the setup. Note that except for the slow drift, no charge noise is observed, indicating no significant vibrations between the two chips. In the case that the drift is solely due to the mechanics of the setup, the gate-heterostructure separation needs to change by \(\Delta d = d \Delta V_8/3V_b = 7.5 \text{ pm}\), using \(\Delta V_8 = 0.75 \text{ mV}\), \(V_b = -2.8 \text{ V}\) and \(d = 84 \text{ nm}\).

**Figure S5: QPC traces at a magnetic field of } B=1.3 \text{ T for assembly A in the main text.** The figure shows the diagonal conductance through the left (black) and right (red) QPC as a function of the gate voltages \(V_{7,10}\) and \(V_{9,12}\), respectively, with the plunger gates set at the depletion point of -
2.2 V. When $V_{7,10}=0$ or $V_{9,12}=0$, $G_d=4e^2/h$, consistent with a filling factor of $\nu=4$ in the bulk at $B=1.3$ T. Interference is observed if both QPC voltages are set on the low voltage side of plateau 3, $V_{7,10}=-1.6$ V and $V_{9,12}=-1.9$ V, as shown in Fig. 3c in the main text. At these gate settings the innermost edge channel (belonging to the fourth Landau level) is fully reflected at the QPC, while the third edge channel has a small backscattering amplitude. The outer two channels belonging to $\nu=1$ and $\nu=2$ are fully transmitted.

Figure S6: QPC traces for assembly B in the main text. (a, b, c, d) Diagonal conductance $G_d$ as a function of gate voltages $V_{9,12}$ for the right QPC of the interferometer at $B=0$, 0.1, 0.3, 0.5 T, respectively. At $V_{9,12}=-3$ V the electrons underneath the gates are depleted. Using a parallel plate capacitor model and the depletion voltage, a gate-heterostructure separation of ~115 nm is derived. At $V_{9,12}=-9$ V the QPC closes. However, due to the large QPC opening of 1.7 µm, quantized conductance is absent at zero magnetic field. In small perpendicular magnetic fields, quantized plateaux resulting from the backscattering of the quantum Hall edge channels are observed. Note that in all traces (a-b) no hysteresis is observed between down (black) and up (red) sweeps of the gate voltages.
Figure S7: Magnetic field and gate voltage period of quantum oscillations as a function of $1/f_T$ for Assembly B, where $f_T$ is the number of fully transmitted edge-channels. (a) The magnetic field periods for different $f_T$ fall on a straight line through zero with a slope of $488.6 \, \mu T/(1/f_T)$. (b) The period in the plunger gate voltage has no obvious dependence on $f_T$. The periods in (a) and (b) are determined from the interference patterns in Fig. 4 (b-g) in the main text after removing the background conductance, which is obtained by a 6th order polynomial fit to the data. The change in the background conductance as a function of gate likely originates from details of the tunnel rates in the QPCs.
Figure S8: Electrostatic potential simulation. A double-layered gate structure can be implemented in the quartz gate-chip, as shown in the cross-section in the top panel. The electron density in the 2DEG can be simulated electrostatically for certain gate voltages. The red curve in the bottom figure shows the density profile in the 2DEG by applying a gate voltage of $V_g = -2.7$ V to the split gates (QPC gates in the interferometer) without implementing the global top gate. The black curve represents the density profile for a geometry with a grounded global top gate. The induced potential landscape is sharper in the latter case, and thus a better control can be achieved. In addition, as discussed in the main text, the top gate also increases the capacitance between gates and island (region enclosed by the interferometer) and can drive the interferometer from the Coulomb-dominated regime into the Aharonov-Bohm regime.

Figure S9: Layout of the GaAs/AlGaAs heterostructure used in this experiment.