

---

This item was submitted to [Loughborough's Research Repository](#) by the author.  
Items in Figshare are protected by copyright, with all rights reserved, unless otherwise indicated.

## Characterization of printed solder paste excess and bridge related defects

PLEASE CITE THE PUBLISHED VERSION

PUBLISHER

© IEEE

VERSION

VoR (Version of Record)

LICENCE

CC BY-NC-ND 4.0

REPOSITORY RECORD

Wilson, Antony R., Andrew A. West, Diana M. Segura-Velandia, Paul P. Conway, David C. Whalley, Lina A.M. Huertas-Quintero, and Radmehr P. Monfared. 2019. "Characterization of Printed Solder Paste Excess and Bridge Related Defects". figshare. <https://hdl.handle.net/2134/4221>.

This item was submitted to Loughborough's Institutional Repository (<https://dspace.lboro.ac.uk/>) by the author and is made available under the following Creative Commons Licence conditions.



**CC creative commons**  
COMMONS DEED

**Attribution-NonCommercial-NoDerivs 2.5**

**You are free:**

- to copy, distribute, display, and perform the work

**Under the following conditions:**

**BY:** **Attribution.** You must attribute the work in the manner specified by the author or licensor.

**Noncommercial.** You may not use this work for commercial purposes.

**No Derivative Works.** You may not alter, transform, or build upon this work.

- For any reuse or distribution, you must make clear to others the license terms of this work.
- Any of these conditions can be waived if you get permission from the copyright holder.

**Your fair use and other rights are in no way affected by the above.**

This is a human-readable summary of the [Legal Code \(the full license\)](#).

[Disclaimer](#) 

For the full text of this licence, please go to:  
<http://creativecommons.org/licenses/by-nc-nd/2.5/>

# Characterization of Printed Solder Paste Excess and Bridge Related Defects

A. R. Wilson, A. A. West, D. M. Segura Velandia, P. P. Conway, D. C. Whalley, L. A. M. Huertas Quintero, R. Monfared.  
Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University  
Loughborough, Leicestershire, LE11 3TU, UK  
A.R.Wilson@lboro.ac.uk

## Abstract

Surface Mount Technology (SMT) involves the printing of solder paste on to printed circuit board (PCB) interconnection pads prior to component placement and reflow soldering. This paper focuses on the solder paste deposition process. With an approximated cause ratio of 50 – 70% of post assembly defects, solder paste deposition represents the most significant cause initiator of the three sub-processes. Paradigmatic cause models, and associated design rules and effects data are extrapolated from academic and industrial literature and formulated into physical models that identify and integrate the process into three discrete solder paste deposition events - i.e. (i) stencil / PCB alignment, (ii) print stroke / aperture filling and (iii) stencil separation / paste transfer. The project's industrial partners are producers of safety-critical products and have recognised the in-service reliability benefits of electro-mechanical interface elimination when multiple smaller circuit designs are assimilated into one larger Printed Circuit Assembly (PCA). However, increased solder paste deposition related defect rates have been reported with larger PCAs and therefore, print process physical models need to account for size related phenomena.

## Introduction

Printed Circuit Assemblies (PCAs) rely on solder to electrically and mechanically interconnect electronic components via a Printed Circuit Board (PCB). Surface Mount Technology (SMT) is the predominant electronic component package format. The prevalent SMT process technology involves the printing of solder paste on to the PCB's SMT pads prior to component placement and solder joint formation via reflow soldering. The ultimate reliability of the solder joint is dependant on not only, (i) the geometry of the provisional solder joint, (ii) but also its long-term mechanical integrity.

Academic literature supports the hypothesis that the mechanical integrity of solder joints may be undermined by rework and that the inherent fatigue resistance of the ensuing repaired joint may be curtailed by the physical degradation potential of rework processes [1, 2, 3, 4]. Physical degradation risks such as, inter-metallic layer growth and joint embrittlement, can be accelerated when rework processes have been manually actuated and are therefore uncontrolled [5]. From an electrical continuity perspective, resultant solder joints can be unequivocally classified as defective if the assembly process has (i) failed to create an interconnection (i.e. an open joint) or

(ii) unintentionally created a short circuit with the bridging of adjacent component leads with solder. However, from a mechanical integrity perspective, if provisional electrically sound solder joints are adjudged geometrically excessive or insufficient, then the repair of any such geometric defects could actually result in replacement joints that are subsequently deemed geometrically acceptable but may have been rendered mechanically less robust than their antecedents. Visual inspection, which is typically manually interpreted and actuated, may compound this risk via the unnecessary reworking of geometrically acceptable inspection misinterpretations – whilst geometrically nonconforming defects may escape this imprecise screening process.

Although open and short circuited joints may have supplemental, potential causes that are unrelated to the print process (e.g. component misalignment, lead bend errors, solder wicking, tombstoning and chip floatation) these electrical failures can also share volumetric deposition related causes with their geometrical defective precursors i.e. insufficient and excessive solder joints.

Insufficient solder joints can be the precursor to open circuits with only the vagaries of the lead-position / deposit-volume aspect ratio differentiating between the two. For example, conforming deposit volumes may produce open circuits if the scale of vertical or horizontal lead position discrepancy prevents any contact between leads and their respective coalesced, molten solder deposits. However if the degree of contact that is required to facilitate full heat transfer to the lead (assuming convection reflow based energy sources) and in turn, promote effective vertical solder flow and satisfactory solder wetting is marginally compromised by nonconformity in either of the aspect ratio's variables, then the resulting defects are usually classified as insufficient joints.

The open circuit and insufficient solder joint scenario of the lead-position / deposit-volume aspect ratio represents a diametrically opposed relationship but logic suggests that if the magnitude of either or both of the ratio variables are projected positively then boundary conditions may be exceeded and short circuits may ensue. The cause and effects relationship of this scenario replicates the basic rules of solder flow and wetting but occurs due to an unintended contact between adjacent leads and deposits. However, the causes of excessive solder joint scenarios are less obvious and worthy of further investigation.

A previously unexplained anecdotal yield reduction has been experienced by an industrial partner to the

authors' research project that can be linked to an effect that is precipitated by larger PCBs. This paper looks to characterise printed solder paste excess and bridge related defects and examine the linkage with the large PCB effect.

**Methodology**

The authors are members of the CLOVES project (Complex Low Volume Electronic Systems) project - DTI Project No: TP//3/DSM/6/I/16333, which includes the following objectives:

to understand the causes of poor first-off performance by statistical analysis of production data and detailed process and process variable profiling;

to develop a software tool that can represent the manufacturing system as comprised of multiple component parts.

In order to satisfy the project's stated objectives, it was originally proposed that the understanding of the causes of poor first-off performance would be facilitated via data mining and statistical analysis of the project's industrial partner production data. However, this source of historical data has proven to contain only assembly defect logs. Defect logs constitute effects data, but to meet the project's first objective and proffer an understanding of the causes of these effects, then data relating to the causation paradigms would be needed. Unfortunately these data are not systematically captured and therefore unavailable within the partner's logs.

As a consequence, the methodology had to be adapted to, (i) an elicitation of causation paradigms from within academic literature which are supported by complimentary empirical data, and then, (ii) the formulation of physical models, which represent the defect opportunities for the representative PCA assembly processes. The software tool will then provide the defect prediction capability for discrete event simulations of the SMT assembly process based on the following three discrete events that constitute the paste deposition sub-process, as shown in Figure 1:

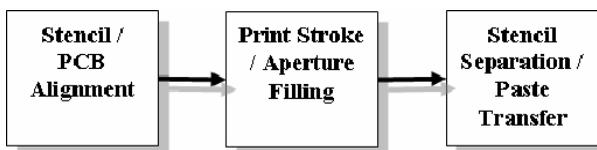


Figure 1 – The Discrete Events of the Solder Paste Deposition Sub-process

Although this methodology is constrained by the gamut of published academic research with accompanying empirical results, the supporting data is quantitative, scientifically sanitised (i.e. peer reviewed) and therefore less vulnerable to human assumptions.

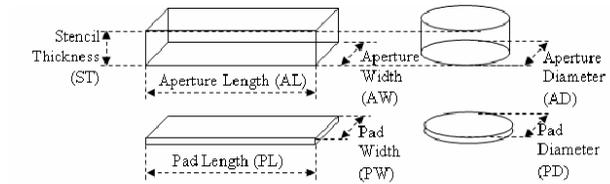
**Findings**

Effects data presented within individual academic studies [6, 7, 8] were elicited to generate stencil aperture design paradigms that are based on the following

corroborated aspect ratios and their corresponding, validated design rules – also see Figure 2:

Aspect Ratio (AR) = Stencil Thickness (ST) / Aperture Width (AW) or Aperture Diameter (AD)

Area Aspect Ratio AAR = Pad / Paste Contact Area (AL\*AW) or (π \*AD/2)<sup>2</sup> divided by the aperture wall surface aspect area (AL\*AW\*2)\*ST or (π \*AD)\*ST



Rule Name	Rule	Rule Name	Rule
Stencil Aperture Aspect Ratio (AR)	AW or AD / ST => 1.5:1	Stencil Aperture Area Aspect Ratio (AAR)	(AL*AW) or (π *AD/2) <sup>2</sup> / (AL*AW*2)*ST or (π *AD)*ST => 0.6:1

Figure 2: AR and AAR Aperture Design Rules

Using the convention given in Figure 2, aperture volume can be formulated as AL \* AW (or AD) \* ST. The transfer ratio (TR) of a given solder deposit can be extrapolated by dividing the measured volume by the theoretical volume (which is equitable with the aperture's volume). Assuming neutral rheological effects, the aperture's release characteristics are determined by a combination of the paste's cohesive bonding to the SMT pad and its internal tensile resistance, which must prevail over its attraction to the aperture wall and the consequential shear resistance experienced whilst under tensile load i.e. during stencil / PCB separation. This relationship explains the aperture design related release characteristic that contribute to negative-value transfer ratios. However, within paradigms which assume that full contact is made between stencil aperture and SMT pad and that a perimeter gasket seal endures, positive-value transfer ratios remain inexplicable.

Poon and Williams, [9] provide testimony to the possibility of the previously unacknowledged phenomenon of positive-value transfer ratios and excess deposit nonconformities. Via its volumetrically scanned nonconformity data and correlated defect rates, they also confirm a cumulative positive-value effect, which is exaggerated by elevated ambient temperatures, but only negated by in-cycle remedial processes such as automated, underside stencil cleaning.

Height only measurement of paste deposits may be capable of detecting the effects of scooping (i.e. paste loss through squeegee blade deflection within the aperture and subsequent scavenging of the upper surface of the deposit – see Figure 3) but it will not detect residual paste that is retained by the aperture wall. It therefore obscures the effects of poor paste release.

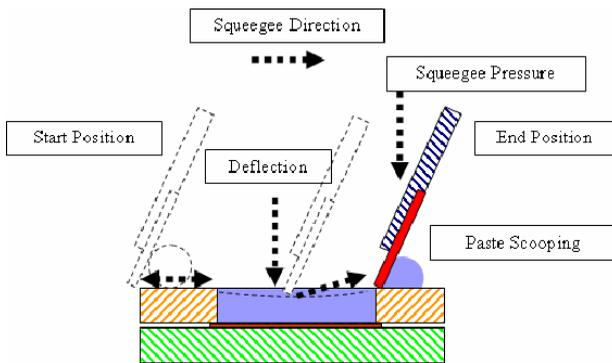


Figure 3: The Scooping Effect

Volumetric scanning is required to differentiate between the causes of negative transfer ratios that would not be apparent via exclusive height measurement methods. For this reason, only the correlating data, which was extrapolated from academic studies that utilised volumetric scanning equipment, was used to formulate the physical models.

### Discussion

By definition, transfer ratios must possess cumulative tendencies. For example, when transfer ratios are less than 100% and deducting the effects of scooping, any further discrepancies must be attributable to retention of residual paste within the aperture. This residue, if uncorrected by remedial action (i.e. effective stencil cleaning), will compound the aperture's already compromised release characteristics. The effective aperture width will decrease as the residue adheres to the walls; further compromising the aspect ratio over successive prints. Hence, a cumulative negative-value transfer ratio will successively reduce the aperture volume and exaggerate the release inefficiencies, ultimately resulting in total aperture blockage.

Given the increased propensity for their electrical detection, reactive stencil cleaning is a more probable consequential scenario of precursory open circuits. Nevertheless, it should be possible to predict proactive cleaning regimes that mitigate the risk of the negative-value, cumulative transfer ratios that equate to insufficient deposit volumes. Poon and Williams [9] recommend a provisional 95% minimum negative-value ratio, thus providing a reasonable benchmark.

Assuming coplanar contact between (i) squeegee and stencil, and (ii) stencil and PCB, transfer ratios that are greater than 100% can only be explained by a loss of aperture / SMT pad gasket seals. Lateral misalignment would seem to be the most likely root cause in circumstances where incidents of excessive solder joints co-inside with localised concentrations of excess deposit, related short circuits. This would explain the project partner's anecdotal defect clustering, which was more prevalent where fine pitch packages are located at the extremities of large PCBs.

Once the gasket seal has been breached, the vector of the force that generates the scooping effect is more likely

to push the paste into the resultant spaces between stencil and PCB that lie within the path of the vector. These gaps will occur due to the stand-off created by the pad to substrate height differentials – see Figure 4.

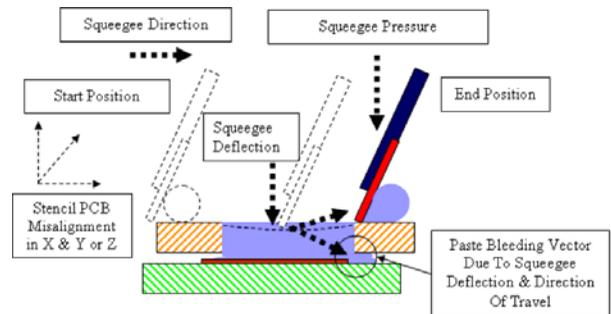


Figure 4: The Bleeding Effect

The magnitude of the pad to substrate height differentials will be a function of the copper thickness plus the specified surface finish. Unless the application requires a high current carrying capacity that will require a greater weight of copper, the average PCB will have a copper cladding / plating depth of 35.5 microns [10]. A typical surface mount compatible flat finish, such as, electro-less nickel / immersion gold (ENIG) will add another 6 to 13 microns [11]. A preference for optimal solderability over pad flatness may require the accommodation of fused Sn / Pb that has been hot air solder levelled (HASL). This surface finish will vary in height across a pad by between 2 to 25 microns [12]. The total pad height differential (herein referred to as PHD) could subsequently vary between 27 and 60 microns. Given that the  $AR < 1.5:1$  rule becomes unviable for FPT (fine pitch technology) geometries at stencil thicknesses that exceed 125 microns, the PHD can easily equate to a significant percentage of the overall stencil thickness (i.e. approximately 35 to 50%).

The potential to breach Poon & Williams' [9] 115% recommended upper limitation for provisional positive-value transfer ratios is exaggerated by high percentage PHDs. Also, a cumulative effect becomes probable via a residue transfer mechanism between successive prints that is similar to the one that accumulates paste in apertures.

It could be argued that this gap may be partially occupied, and therefore lessen the potential for post reflow defects, if the pad pattern is fully defined by the solder resist mask (a polymer coating that is applied to the substrate surface to protect the copper tracks and repel unwanted dispersed solder). However, a counter argument that accounts for the influence that solder resist has on bleeding can be derived from the fact that the limits of solder resist registration accuracy make the chances of achieving resist-free pad definitions for 0.5 mm pitch geometries and below, at best marginal. The probability of resist encroachment onto the pad will make gap exaggeration a more likely outcome. This assessment is corroborated by a CLOVES project partner who has

affected a defect reducing corrective action at the PCB layout design stage, via the elimination of the resist webs that enclose ultra FPT pads.

If the deposit registration error is greater than the aperture reduction it will effectively reduce the gap between deposit and adjacent pad and promote unintended contact with a neighbouring component lead, thus, increasing the probability of a post-reflow short circuit. This two dimensional error would also be expanded into the third dimension as the PHD gap fills, thus facilitating provisional positive-value transfer ratios and the probability of post-reflow excessive solder joints – see Figure 5.

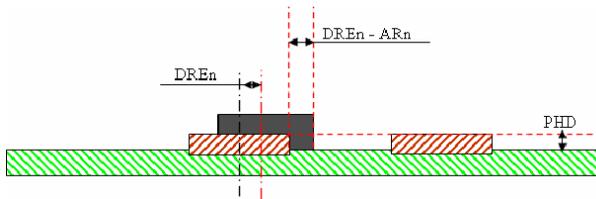


Figure 5 – Deposit Bridge & Excess Model

This provisional positive-value scenario may also be compounded by a cumulative effect. As is the case with negative-value accumulation, the accretion of excessive and bridged related defects must be caused by residue build-up on stencil surfaces. However, rather than the residue being retained within the aperture and reducing its volume, the positive-value accumulation must be via surface residue transfer between successive prints. This phenomenon could be explained by a residue that is deposited on the underside of the stencil webs that separate the FPT apertures as a result of paste bleeding – see Figure 4. The causation paradigm is supported by the fact that the Poon and Williams’ [9] positive-values return to nominal with each stencil cleaning cycle.

The following paradigms and rules are proposed for the physical models:

Deposit Registration Error & Bridging Model:

$$DBPn = \frac{DREn}{PPG}$$

or,

for rectilinear pads,

$$DBPn = \frac{BDEn \times PCn}{CP - PW}$$

for round pads,

$$DBPn = \frac{BDEn \times PCn}{CP - PD}$$

where,

- DBPn = X or Y deposit bridge potential ratio
- DREn = X or Y deposit registration error
- PPG = pad to pad gap
- BDEn = X & Y board dimensional error
- PCn = X & Y component position from PCB centroid
- CP = component pitch

Deposit Bridging Rule:

If  $DREn \leq ARn$  then DRDP bridging possibility = 0%

where,

ARn = X & Y aperture reduction dimension

Deposit Registration Error & Excess Model:

for rectilinear pads,

$$DEPn = \frac{DV + ((DREn - ARn) \times AL) \times PHD}{AW \times AL \times ST}$$

for round pads,

$$DEPn = \frac{DV + (\pi((AD - ARn)/2)^2 - \pi((PD - DREn)/2)^2) \times PHD}{AW \times AL \times ST}$$

where,

- DEPn = X & Y deposit excess potential ratio
- TR = transfer ratio
- AV = aperture volume
- DV = deposit volume
- PHD = pad height differential
- CT = copper thickness (e.g. 1 oz Copper / inch<sup>2</sup> = 0.036 mm)
- SFT = surface finish thickness (e.g. ENIG = 0.006mm to 0.013 mm)

Deposit Registration Error Volume Rule:

If provisional TR > 115% then SCF (stencil cleaning frequency) = 100%

The anecdotes of a disproportional increase in excessive and bridged solder joints, which are clustered around FPT components that are located at the extremities of large PCBs suggests a dimensional mismatch that results in a lateral misalignment between stencil apertures and SMT pads. Further analysis of the PCBs that exhibited the phenomenon highlighted an unexpectedly large, dimensional error that increased proportionally over distance. The corresponding solder paste stencil did not incur a cumulative dimensional error. The potential for this type of mismatch is illustrated in Figure 6.

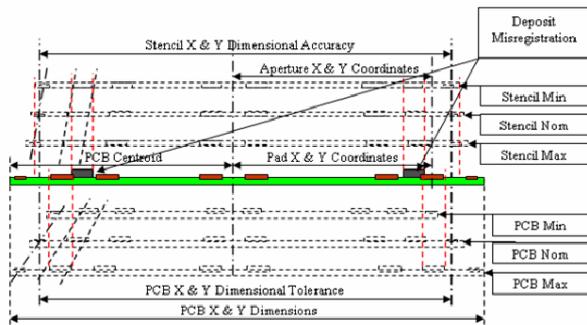


Figure 6: PCB Stencil Dimensional Mismatch

The stencil / PCB alignment systems of automated SMT printers that use vision systems to locate and align the stencil and PCB can also check for dimensional errors whilst attempting a best-fit lateral alignment – i.e. a compromised solution that minimises their effect but does not compensate for the original dimensional errors. Unless programmed about an alternative, user defined fulcrum, the best-fit alignment will be centred about the PCB's CAD data centroid. Thus, the location of FPT sites at the extremities of large PCBs, will amplify dimensional mismatches, effectively reducing the post-alignment clearance between stencil apertures and the nearest neighbour of their corresponding PCB interconnection pad.

This paradigm provides a possible explanation for the causes of the large PCB cumulative effects that generate both (i) deposit registration nonconformities (ii) breached gasket seals and positive-value transfer ratio nonconformities.

Lotosky et al. [13] describe the lateral misregistration paradigm and provide data and a corrective action that reduced print deposit related defects by an average of 43% by remaking the stencil with a, 0.5 microns per millimetre, negative-scaled compensation factor. It should be noted that their application (i.e. automotive engine-control modules) required a specialist technology substrate construction, with a 0.175 mm thick flexible FR-4 circuit laminated onto a 2 mm thick rigidizer. Therefore, the Lotosky et al.'s [13] negative-error factor (0.5 microns per PCB millimetre in X and Y) can not be adopted as a generic, dimensional error rule. Rahn [14] suggests that PCBs can shrink during pre-production storage and that stencils can stretch during extended usage, an effect that will be exaggerated by off-contact printer set ups and vertical misregistration. However, the CLOVES project partner's anecdotal evidence identified a positive PCB dimensional scaling error (i.e. a BDEn) that was found to be the cause of the increased bridging and excess effect.

The Lotosky et al.'s [13] corrective action (i.e. the remaking of the stencil with lateral scaling-error compensation) assumes a constant dimensional error. This predictability may be feasible given their specific substrate construction, but whilst Rahn [14] has suggested time based dimensional shrinkage vagaries, the partner

anecdote has illustrated the possibility of stretched substrate scaling errors.

## Conclusions

The conflicting reports of substrate shrinkage and stretching suggest that, the remanufacturing of stencils with scaled BDEn compensation, as a process orientated corrective action could not provide a generic solution for large PCA dimensional scaling errors. Multiple variants might be required and repetitive coordinate measurement analysis would become mandatory as part of a costly individual PCB pre-screening and error matching process.

A product-design based resolution would be much more cost effective, if actuated at the PCB layout design stage. If the Lotosky et al. [13] scaling error were apparent in the CLOVES project industrial partner's design that locates 0.5 mm pitch packages at 200mm from the PCB's centre, the error would equate to 1.0 mm, or alternatively a two lead pitch mismatch. For a scaling error that was only one tenth of the Lotosky et al. [13] findings, the mismatch would still be sufficient to breach the gasket seal of a 10% reduced aperture, thus promoting paste bleeding, increasing the probabilities of excessive and bridged deposits and instigating a 100% stencil cleaning frequency requirement.

In the scenario where dimensional scaling tolerances were considered at the design stage, aperture reductions could be calculated and matched accordingly via the proposed software tool development; thus guiding the designer to relocate the component in a less sensitive (i.e. more central) position, or alternatively recommending a substitute SMT package style of equitable footprint but large pitch, e.g. a coarser pitch area array as an alternative to a FPT peripheral leaded device. Also, alternative stencil thickness recommendations could be provided that are based on transfer ratio physical models and minimum aspect and area aspect rules. This functionality could enable interactive design-for-manufacture guidance during PCB layout and facilitate synchronous product and process design.

## References:

1. Nguty, T. A., Ekere, N. N., Philpott, J. D., Jones, G. D., "Rework of CSP: the Effect On Surface Intermetallic Growth", *Soldering & Surface Mount Technology*, Vol. 12 No.3 (2000) pp 35-38
2. Garrison, A., Lee, M., Park, H. S., and Todd, N.L., "How Much Rework is Too Much?: the Effects of Solder Joint Rework on Plated Through Holes in Multilayer Printed Wiring Boards", *Soldering & Surface Mount Technology*, February, No. 19 (1995) pp 48-51.
3. Lau, J., Leung, S., Subrahmanyam, R., Rice, D., Erasmus, S. and Li, C.Y., "Effects of Rework on the Reliability of Pin Grid Array Interconnects", *Circuit World*, Vol. 17, No. 4 (1991), pp 5-10.

4. Hutchins, C. L., "Reliability vs. Processing Temperatures", *Surface Mount Manufacturing*, December, 1995, pp 16-18.
5. Lea, C., "The Harmfulness of Reworking Cosmetically Defective Solder Joints", National Physical Laboratory, Teddington, Middlesex, England (1990).
6. Pan, J., Tonkay, G. L., Storer, R. H., Sallade, R.M., Leandri, D.J., "Critical Variable of Solder Paste Stencil Printing for Micro-BGA and Fine-Pitch QFP", *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 27, No. 2 (2004), pp 125-132.
7. Mannan S. H., Ekere, N. N., Lo, E. K., Ismail, I., "Predicting Scooping and Skipping in Solder Paste Printing for Reflow Soldering of SMT Devices", *Soldering & Surface Mount Technology*, October, No. 15 (1993), pp 14-17.
8. Durairaj R., Nguty, T. A., Ekere, N.N., "Critical Factors Affecting Paste Flow During the Stencil Printing of Solder Paste", *Soldering & Surface Mount Technology*, Vol. 13, No. 2 (2001), pp 30-34.
9. Poon, G. K. K., Williams, D. J., "Characterisation of a Solder Paste Printing Process and its Optimisation", *Soldering & Surface Mount Technology*, Vol. 11, No. 3 (1999), pp 23-26.
10. Lea, C., "A Scientific Guide to Surface Mount Technology", Electrochemical Publications Limited, (Ayr, Scotland,1988).
11. Association Connecting Electronics Industries, IPC-4552/02 "Specification for Electroless Nickel/Immersion Gold (Enig) Plating for Printed Circuit Boards", IPC, (Northbrook, IL, USA, 2002).
12. Klein Wassink, R. J., "Soldering in Electronics", Electrochemical Publications Limited, (Isle of Man, UK, 1989).
13. Lotosky, P., Murphy, M., Pearson, R., Tesch, M., "Using Stencil Design to Reduce SMT Defects", *SMT*, April 2006, pp 34-36.
14. Rahn, A., "Pastes, Stencils and Process Control", *SMT*, February 2006, pp 28-34.