A W-band balanced power amplifier using broadside coupled strip-line coupler in SiGe BiCMOS 0.13-μm technology

A W-Band Balanced Power Amplifier Using Broadside Coupled Strip-Line (BCSL) Coupler in SiGe BiCMOS 0.13-μm Technology

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***Abstract*— Load-variation insensitivity for impedance matching between power amplifiers (PAs) and transmitted antennas contributes to challenge the design of millimeter-wave wireless systems. In this paper, a W-band two-way balanced power amplifier (PA) based on a compact quadrature coupler with broadside coupled strip-line (BCSL) as the core section has been presented to enhance the load-variation insensitivity and stability. By utilizing the proposed coupler topology, the proposed coupler obtains broadband performances with low amplitude and phase imbalance. The designed W-band PA achieves higher power-added efficiency (PAE) and saturated output power P_{sat} over wide frequency bandwidth. The proposed W-band balanced PA is implemented in a 0.13-μm SiGe BiCMOS process and achieves a measured P_{sat} of 16.3 dBm and a peak PAE of 14.1% at 100 GHz under 1.6-V power supply. The measured P_{sat} with 1-dB bandwidth is from 91 to 102 GHz. The measured results present the feasibility of the compact quadrature coupler. The total chip area (with pads) is 0.64 mm^2, where the size of the proposed quadrature coupler is only 0.04 mm^2.**

***Index Terms*- SiGe, W-band, quadrature coupler, broadside coupled strip-line (BCSL), balanced power amplifier.**

I. INTRODUCTION

Millimeter-wave (mm-Wave) communication systems with a high-speed data rate of multi-Gigabit per second (Gb/s) have received significant attentions in recent years [1]-[7]. The W-band (75 to 110 GHz) is considered as a good choice with its wide available bandwidth for Gb/s wireless communications or several other applications such as high-resolution sensing [8]-[11]. As one of the most challenging components in W-band wireless systems, W-band power amplifiers (PAs) are expected to be designed with high efficiency and output power. To achieve the high performance, several excellent PAs have been reported in [12]-[22] taking the advantages of nanoscale CMOS technologies. Recently, the SiGe BiCMOS technology has been drawn significant attentions to the high speed performance of heterojunction bipolar transistors (HBTs), which is believed to be an excellent candidate for high output power millimeter-wave (mm-Wave) wireless applications [23]-[26].The breakdown voltage in a standard 0.13-μm SiGe BiCMOS dictates a nominal supply voltage of approximate 1.7 V with high current density and cut-off frequency f_T[27]. Therefore, the SiGe BiCMOS technology is ideal for power amplifier design to obtain good performances at mmWave or sub-mmWave band.

Notably, the system-on-chip (SoC) technology using antenna-in-packaging brought a promising era for a solution of fully-integrated mmWave transceiver frontend [28]-[29]. However, it turns out to be a particular challenging and interesting work for the antenna to be treated as the load of the PA, especially at mmWave bands. It is noted that PA can be sensitive to the variations in load impedance, which might affect the input and output performances of the PA, and further degrade the transmitted power of the systems. This issue turns out to be particular challenging in mm-Wave system as the frequency goes high. As a promising solution, the balanced PAs [30]-[31] are believed to have inherent load-variation insensitivity for load impedance and matching. However, the balanced PA technique in mm-Wave PA design has rarely been reported. A typical balanced PA consists of two quadrature couplers and two identical single-ended PAs. There are two parts of the on-chip balanced PA design should be considered. The first one is tradeoff between the chip size and power losses for the balanced PA. For the on-chip passive devices [32]-[36], it should own the minimal power losses and compact circuit size. However, it turns to be difficult to implement the on-chip power combining circuits for PA using the lumped inductors/capacitors or transformer. This is mainly because, in general, though the size of the lumped inductors/capacitors or transformer are smaller than transmission line, the quality factor of transmission line is higher than lumped inductors/capacitors or transformer at high frequency. Normally, the transformer and additional capacitors are implemented for conventional on-chip couplers [33]-[34].Therefore, the transmission line of broadside coupled strip-line (BCSL) is used in this design to minimize the chip size and power loss. Secondly, the 90° phase difference bandwidth of quadrature coupler could determine the

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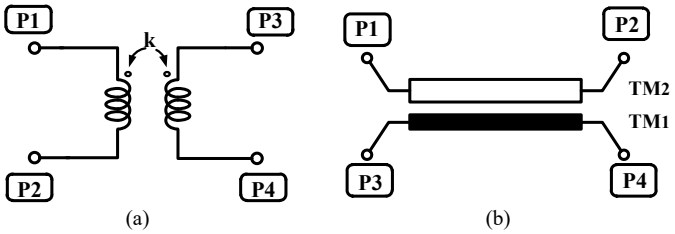

Fig.1. Schematics of (a) ideal coupled-inductors and (b) ideal four-port broad-side coupling line (BCSL).

performances of the balanced PA. However, the conventional approach [33]-[34] using the transformer and additional capacitors has limited operation bandwidth especially 90° phase difference bandwidth at high frequency. Theoretically, in this design, applying BCSL with additional lumped inductors and capacitors, the phase difference bandwidth of the quadrature coupler is independent of the frequency. Hence, this proposed topology of quadrature couple could be used in balanced PA design at high frequency band such as V-band or W-band.

In this paper, a W-band balanced power amplifier with compact quadrature couplers is designed. The proposed compact quadrature coupler consists of the broadside coupled strip-line (BCSL) and the lumped inductors and capacitors connected among adjacent ports. The proposed coupling mechanism owns a wideband performance and a minimized phase imbalance response over the entire bandwidth. Furthermore, the coupler is designed using BCSL with miniaturized layout, consequently leading to a reduced signal loss while travelling along the metal lines. The W-band balanced power amplifier has high PAE and saturated output power with unconditional stability over the interested frequency range. Taking advantages of the high Q factor of lumped components and the improved coupling effect of BCSL, the designed quadrature coupler maintains a miniaturized layout and good performance of the balancing circuitry for further pushing up the overall performance of the balanced PA.

This paper is organized as follows: Section II gives the analysis, modelling and implementation of the BCSL in a standard 0.13-μm SiGe technology. The W-band balanced PA design and its post-simulation performances are illuminated in Section III. The measured results of proposed W-band balanced PA are revealed in Section IV while the conclusion is given in Section V.

II. ANALYSIS OF BCSL-BASED QUADRATURE COUPLER

A. Requirement of the Quadrature Coupler

Due to the symmetric geometry of the quadrature coupler, the core is a section of coupled transmission lines that support two different propagation modes of common-mode and differential-mode [37]. Coupled transmission line is one of the circuit structures for the quadrature coupler. If the coupled transmission line satisfies symmetrical of two principle axis

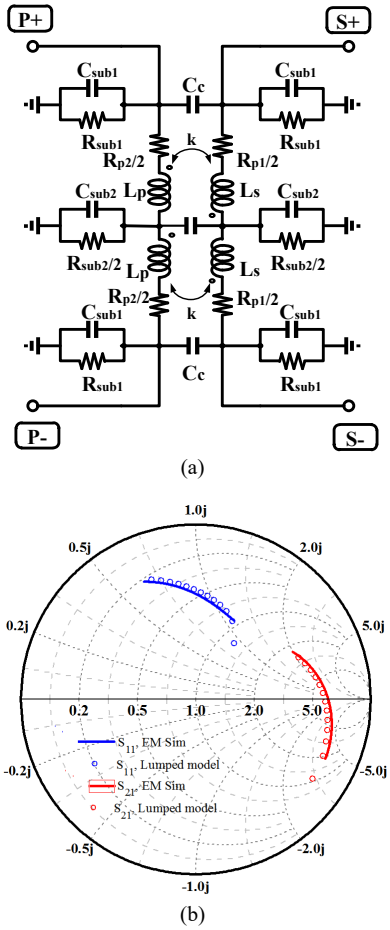

Fig.2. (a) Lumped-element model of BCSL (b) Comparison of four-port S-parameters of BCSL obtained using lumped-element model and HFSS EM simulations.

and supporting two different propagation modes, it is possible to be a quadrature coupler. However, edge coupled microstrip lines are normally used to implement the conventional quadrature coupler in Print-Br oad-Circuit (PCB) technology. This circuit structure is not suitable to be utilized in on-chip coupler design due to the inherent large circuit layout. The transformer satisfies being used for a conventional quadrature coupler excepted that it supports either differential-mode or common-mode signal. The four-terminal transformer could support the differential propagation mode but it is not considered as a coupler. Therefore, some other additional four reactive components supporting the common mode is required. In this design, it uses the broadside-coupling line (BCSL) to implement the core section of the proposed quadrature coupler instead of on-chip transformer to support the differential-mode in SiGe technology.

B. BCSL with Differential Mode

The coupled-inductors is widely used in analog integrated RF circuits as shown in Fig. 1 (a). The ideal complete set of S-parameters of the coupled-inductors with tight coupling is presented in (1).

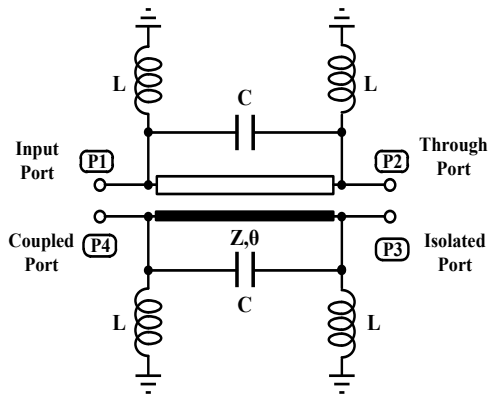

Fig.3. Schematics of proposed coupler with BCSL.

$$\begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix} = \begin{pmatrix} \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} \\ -\frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix}. \quad (1)$$

The BCSL as coupled-inductors supports differential-mode transmission, which allows differential signals to pass through and fully suppresses common-mode signals. It can be observed by conversing (1) to mixed-mode S-parameter. The common-mode and differential-mode S-parameters are given by:

$$\begin{pmatrix} S_{CC11} & S_{CC12} \\ S_{CC21} & S_{CC22} \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \quad (2)$$

$$\text{and} \begin{pmatrix} S_{DD11} & S_{DD12} \\ S_{DD21} & S_{DD22} \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \quad (3)$$

From (2), $S_{CC11}= S_{CC22}=1$ results in perfect common-mode signals termination by opening circuit and $S_{CC21}= S_{CC12}=0$ results in zero transmission. From (3), $S_{DD21}= S_{DD12}=1$ results in perfect differential-mode signals transmission and $S_{DD11}=S_{DD22}=0$ results in zero reflection from the coupled-inductors.

To further reduce the on-chip circuit areas, in this design, the broadside-coupling line (BCSL) structure is used to be as the core section to support differential-mode transmission as shown in Fig. 1(b). Practically, the parasitic effects from silicon process on BCSL should be taken into considerations. The lumped model used for the coupled-inductors is based on the model presented in [38] which is shown in Fig. 2(a). There are some parameters of the model, including the primary inductors (L_P and L_S), the parasitic coupling capacitors and the parasitic resistors, have been considered and simulated in ADS. The coupling coefficient (k), substrate capacitance (C_{sub1}) and resistance (R_{sub1}) have been fit to electromagnetic (EM) simulations of the BCSL in *HFSS*. As can be seen in Fig. 2(b), there is a very good agreement between the lumped-element model and the EM simulation over a broad frequency range from 80 GHz to 120 GHz.

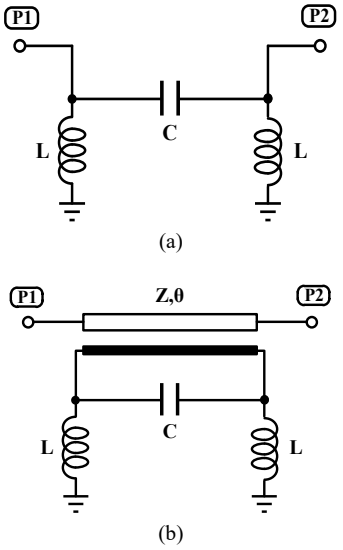

Fig.4. Half circuits of proposed coupler with BCSL (a) Even-mode and (b) Odd-mode.

C. Analysis of Proposed Quadrature Coupler Based on BCSL

The circuit schematic of the proposed quadrature coupler with BCSL is illustrated in Fig.3. Due to the usage of BCSL section and reactive elements, the total circuit could be as the quadrature coupler. The BCSL section shown in Fig.2(b) has the characteristic impedance Z and the electrical length θ, respectively. The two capacitors have a capacitance of C while the four inductors have the same inductance of L. Since the symmetrical network of the proposed coupler shown in Fig. 3, it could be divided into two equivalent half circuits as shown in Fig. 4. To simplify the analysis and reduce the circuit size of BCSL, the electrical length θ is assumed to be equal to 90°. The characteristics of these two half circuits could be obtained by the following analysis.

The *ABCD* parameters of the equivalent circuits for even- and odd-mode excitations can be obtained as

$$\begin{bmatrix} A_e & B_e \\ C_e & D_e \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{sC} \\ \frac{1}{sL} & 1+\frac{1}{s^2LC} \end{bmatrix}, \quad (4)$$

$$\begin{bmatrix} A_o & B_o \\ C_o & D_o \end{bmatrix} = \begin{bmatrix} \frac{Z(1+s^2LC)+sL(Z+Z_0)e^{js}}{sL[ZsC+(Z+Z_0)e^{js}]} & \frac{Z}{ZsC+(Z+Z_0)e^{js}} \\ \frac{2sL+Z}{s^2L^2[ZsC+(Z+Z_0)e^{js}]} & \frac{Z(1+s^2LC)+sL(Z+Z_0)e^{js}}{sL[ZsC+(Z+Z_0)e^{js}]} \end{bmatrix} \quad (5)$$

By using the ABCD parameters, the even- and odd-mode scattering-parameters can be obtained as

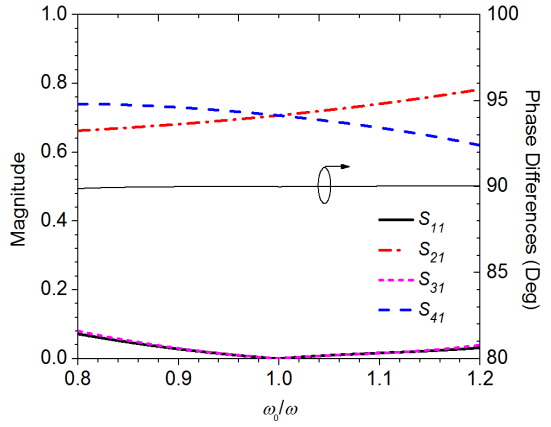

Fig.5. Theoretical results of proposed coupler with S-parameters and phase imbalances.

$$\begin{cases} S_{11E} = \dfrac{A_eZ_0 + B_e - C_eZ_0^2 - D_eZ_0}{A_eZ_0 + B_e + C_eZ_0^2 + D_eZ_0} \\ S_{21E} = \dfrac{2Z_0}{A_eZ_0 + B_e + C_eZ_0^2 + D_eZ_0} \\ S_{22E} = \dfrac{-A_eZ_0 + B_e - C_eZ_0^2 + D_eZ_0}{A_eZ_0 + B_e + C_eZ_0^2 + D_eZ_0} \end{cases}, \tag{6}$$

$$\begin{cases} S_{11O} = \dfrac{A_oZ_0 + B_o - C_oZ_0^2 - D_oZ_0}{A_oZ_0 + B_o + C_oZ_0^2 + D_oZ_0} \\ S_{21O} = \dfrac{2Z_0}{A_oZ_0 + B_o + C_oZ_0^2 + D_oZ_0} \\ S_{22O} = \dfrac{-A_oZ_0 + B_o - C_oZ_0^2 + D_oZ_0}{A_oZ_0 + B_o + C_oZ_0^2 + D_oZ_0} \end{cases}, \tag{7}$$

Thus, the total scattering parameters of the proposed quadrature coupler can be determined by

$$\begin{cases} S_{11} = S_{33} = \dfrac{S_{11E} + S_{11o}}{2} \\ S_{22} = S_{44} = \dfrac{S_{22E} + S_{22o}}{2} \\ S_{21} = \dfrac{S_{21E} + S_{21o}}{2} \\ S_{31} = \dfrac{S_{21E} - S_{21o}}{2} \\ S_{41} = \dfrac{S_{11E} - S_{11o}}{2} \end{cases} \tag{8}$$

Theoretical scattering parameters of a quadrature coupler are

$$S_{11} = S_{22} = S_{31} = 0 \tag{9a}$$

$$|S_{21}| = |S_{41}| = \frac{1}{\sqrt{2}} \tag{9b}$$

Here, scales of the S_{11}, S_{22}, and S_{31} are magnitude. The power ratio is used to define the power dividing ratios of proposed coupler between port 2 and port 4. While both (9a) and (9b) are satisfied while the equations (6-9) are considered, the following conditions can be obtained as

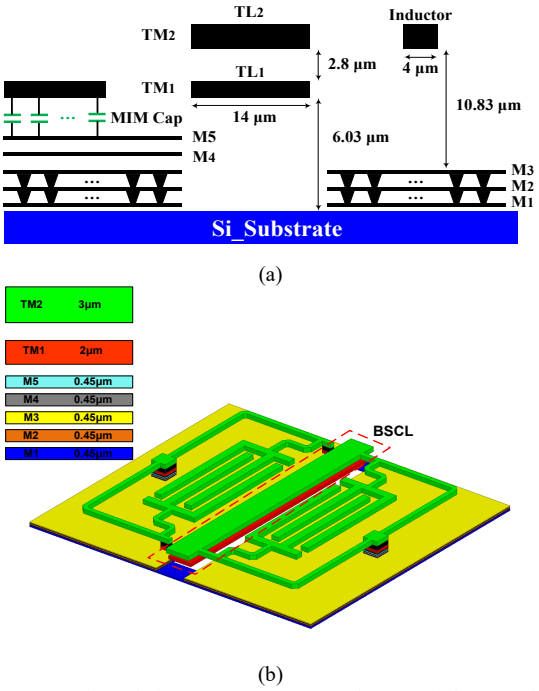

Fig.6. (a) Cross view of SiGe 0.13um process and BCSL, inductors with M_3 as ground plane (b) EM 3D layout of proposed quadrature coupler with BCSL.

$$\begin{cases} (A_e - A_o) + (D_e - D_o) = 0 \\ (A_e - A_o) - (D_e + D_o) = 0 \\ (B_e - B_o) + Z_o^2(C_e - C_o) = 0 \\ (B_e + B_o) - Z_o^2(C_e + C_o) = 0 \end{cases} \tag{10}$$

The condition (10) can be rewritten as

$$\begin{cases} A_e = D_o \\ A_o = D_e \\ B_e = Z_o^2 C_o \\ B_o = Z_o^2 C_e \end{cases} \tag{11}$$

Based (4), (5) and (11), we can obtain the following mathematical relationship:

$$L = \frac{Z(2+\sqrt{2})}{\omega} \tag{12a}$$

$$C = \frac{1}{\omega Z(2+\sqrt{2})} \tag{12b}$$

After obtained the values of the additional inductors L and capacitors C, the magnitude imbalance could be given by

$$\left|\frac{S_{21}}{S_{41}}\right| = \frac{\omega_0}{\omega}. \tag{13}$$

The ω_0 is defined as the center frequency. Theoretically, the magnitude imbalance is straightly proportional to ω, which is the rarely factor to limit the power dividing ratio bandwidth.

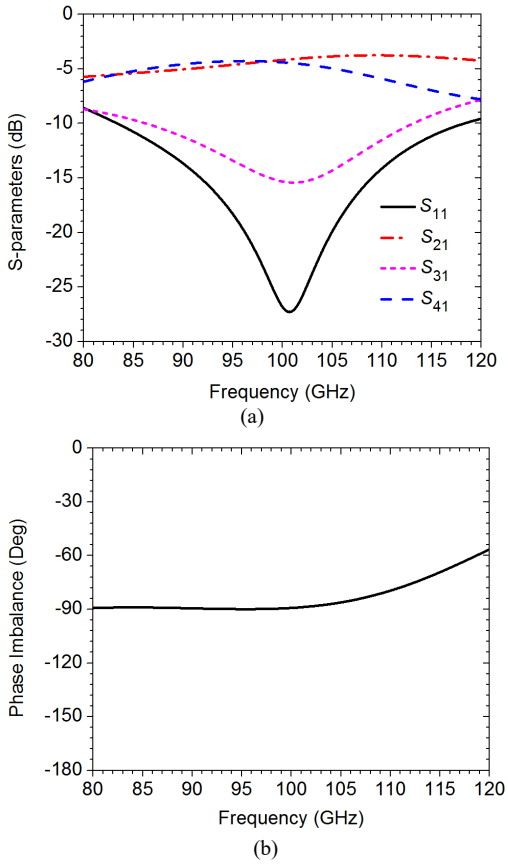

Fig.7. Full EM-simulated results of proposed coupler with (a) S-parameters and (b) Phase imbalances.

The phase difference is given by

$$\left|\angle S_{21} - \angle S_{41}\right| = 90^{o} \tag{14}$$

The phase difference is 90° that is independent of frequency. The calculated results of the ideal proposed quadrature coupler have been illustrated in Fig.5.

D. Implementation of Proposed BCSL-Based Quadrature Coupler in 0.13-μm SiGe

The proposed quadrature coupler is implemented by 0.13-μm SiGe technology in this design. The thick metal layers of Top Metal 2 (TM_2) and Top Metal 1 (TM_1) are used to implement the BCSL on chip. Since the BCSL is used to support the differential transmission signals, the virtual ground exits between TM_2 and TM_1. Therefore, other metal layers under the BCSL area are fully removed to avoid the unnecessary impact. The on-chip inductors of this W-band coupler are implemented by high impedance microstrip line with M_3 used as the ground plane. The layout of BCSL and on-chip inductors are shown in Fig.6(a). Notably, the interdigital structures are applied on TM_2 to implement the on-chip capacitors in this design. The 3D layout of the proposed quadrature coupler is illustrated in Fig. 6(b).

The proposed quadrature coupler is designed and optimized using EM simulation tool *HFSS*. In this proposed coupler, an on-chip interdigital capacitor is connected to the BCSL with vias between TM_2 and TM_1. The full-EM simulated results of the proposed coupler are shown in Fig.7. The simulated insertion loss of the proposed coupler is less than 4.3 dB at 80-110 GHz, and the return loss is larger than 10 dB at 85-115 GHz. The amplitude and phase imbalance are 1.5 dB and 5°, respectively, up to 110 GHz.

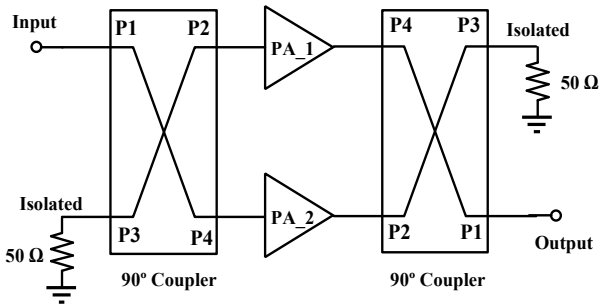

Fig.8. Architecture of Balanced Power Amplifier.

III. W-BAND BALANCED POWER AMPLIFIER USING PROPOSED QUADRATURE COUPLER

A. Principle of Balanced PA

The balanced PA owns some advantages such as load-variation insensitivity, enhanced stability, output power combining, wide bandwidth, and enhanced input and output matching [30]-[31]. The load variation insensitivity is important for mm-Wave PA design. The imprecise load impedance matching results in performance degradation of the PAs.

In Fig.8, the input signal is split into two parts by the input coupler with an equal power dividing ratio with 90° phase difference and delivered to the ports P_2 and P_4, respectively. These two separated signals are amplified by ***PA_1*** and ***PA_2*** and then combined by the output coupler with reversed 90° phase difference to get the output power. Reflected signals would be produced due to the impedance mismatch. After through the input 90° coupler once again, the reflected signals of two ways appear at P_1 port owns the 180° phase difference, which would obtain the unconditionally matching level [31] at the *Input* by cancelling each other. What's more, the reflected signals are superimposed with 0° phase difference at the P_3 *Isolated* port which should be terminated by a 50 Ω load. It owns the same principle at the output port of the balanced PA with better impedance matching. Due to the parallel arrangement of the proposed PAs, the gain of the balanced PA is the same as a single-ended one. Even though the load impedance of each single-ended PA mismatches with a very high gain in the balanced PA, the stability of the balanced PA can be improved. Therefore, in the balanced PA design, the load impedance matching requirement of each single-ended PA can be relieved to obtain better and reliable performances. Additionally, even if one of the PAs is broken in the on-chip balanced PA, the PA can still work with a reduced gain by 6 dB.

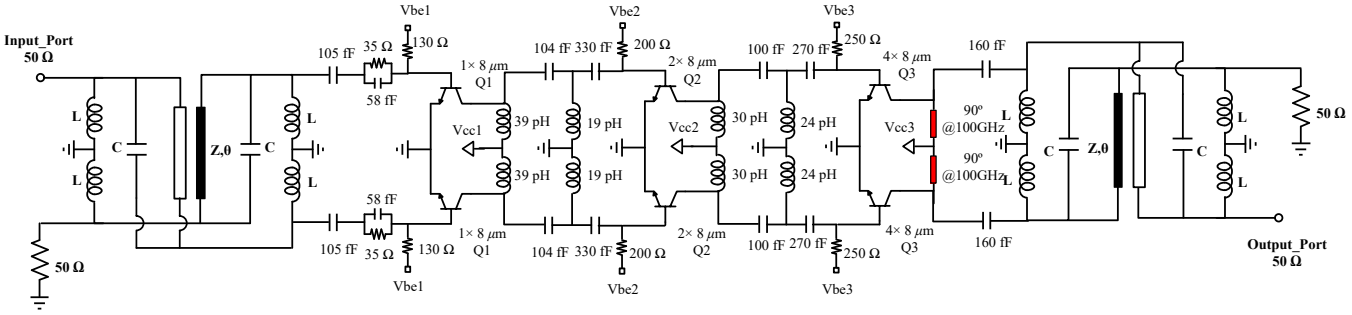

Fig.9. Circuit schematic of W-band balanced power amplifier with proposed quadrature coupler implementation in 0.13μm SiGe.

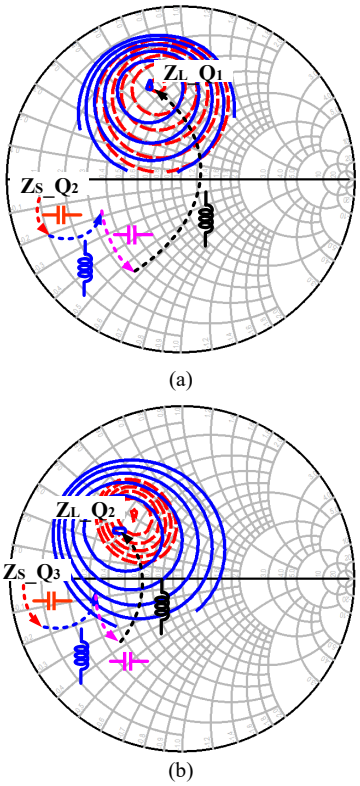

Fig.10. Inter-stage matchings for 3-stage PA (a) from Q_1 to Q_2 and (b) from Q_2 to Q_3.

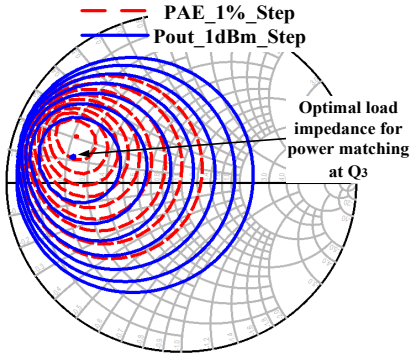

Fig.11. Simulated output power P_{out} and PAE contours versus load impedance presented at Q_3.

B. Architecture of Proposed Balanced PA

Fig. 9 presents the schematics of the proposed W-band balanced PA with BCSL-based quadrature coupler. A quadrature coupler separates the input signal into two paths with 90° phase difference and a same quadrature coupler combines the output for higher delivery power. Both the input and output proposed quadrature couplers are designed with the consideration of input and output impedance matching. To increase gain and enhance output power, a three-stage topology has been adopted in this design. To solve the inter-stage matchings issues raised by the three-stage topology, the T-networks are inserted at Q_1-to-Q_2 and Q_2-to-Q_3, respectively, as of which the matching effects are demonstrated in Figs. 10(a) and (b), correspondingly. Taking a branch of single-ended PA into consideration, the 90° microstrip lines at the collector node of Q_3 is used as RF choke with implementation of the matching network between Q_3 and the output port (50 Ohms). The high impedance microstrip lines and the Metal Insulator Metal (MIM) capacitors are used as inductors and capacitors in inter-stage matching networks, respectively. The EM simulations for the full PA structure implemented in the layout are investigated in this design to ensure parasitic effects are fully considered. V_{CC1}, V_{CC2} and V_{CC3} are the supplies of the first, second and third stage of the proposed PA, respectively. Meanwhile, the V_{BE1}, V_{BE2} and V_{BE3} are three biasing supplies for base nodes of each stage to conveniently tune the proposed PA for performance optimization.

C. Transistor Size and Impedance Matchings

Since the output power is one of the main challenges in W-band PA design, the transistor size in the PA should be carefully considered. In this design, the PA consists of three common-emitter stages in the class AB biasing condition. This proposed PA is fabricated in IHP SG13G2 0.13-μm BiCMOS SiGe HBT technology [27] with device peak f_T / $f$max of around 300/500 GHz. What's more, the breakdown voltages V_{CEO} is 1.6 V. Each bipolar transistor with device size of 8×0.07×0.9 μm^2 is used in this design. The larger-sized transistor owns the higher output power capability. However, the parasitic effects from the transistor layout would increase when the size of the transistor is larger. Moreover, the optimal source and load impedances of the transistor for maximum output power and power-added efficiency (PAE) would change with different sizes of the transistors. Therefore, the optimal size of the transistor should be carefully selected when designing W-band PA. To obtain higher output power and simplify the W-band

PA design process, in this work, we choose the standard active device cells from the foundry PDK. To ensure enough driving power capability, the first- and second-stage transistors, Q_1 and Q_2, consist of 1-parallel and 2-parallel 4 μm standard bipolar cells, respectively. Since the last stage always determines the maximum output power capability of the PA, the third stage power transistor Q_3 is designed using 4-parallel standard bipolar cells. Hence, Q_3 is implemented using four of $8\times0.07\times0.9$ μm^2 transistors connected in parallel to form the 32 μm emitter-length device.

The source impedances of each stage transistor are considered. The lower biasing resistor is used to enhance the I_{BE}, which could improve the output load current with high output power P_{sat}. The source impedances of Q_1, Q_2, and Q_3, are 7-j12 Ω, 5.1-j2.6 Ω, and 3.3-j1 Ω at 100 GHz, respectively. In this design, we choose the biasing resistors (>100 Ω) larger than the source impedances of each stage transistor, as is shown in Fig. 9. The load pull technique is used to optimize the load impedance of the transistor at each stage with a maximum output power at 100 GHz. The optimum load impedance for Q_3 is 10.8-j5.4 Ω with a maximum output power of 17.9 dBm at 100 GHz as shown in Fig. 11. In Fig. 9, the output matching is implemented using the high-pass impedance network and the inductors are absorbed by the proposed quadrature coupler at the output port. Similarly, the input- and inter-stage-matchings are also implemented using the inductor and capacitor circuits. The MIM capacitors are used from foundry standard PDK. Inductors are implemented using TM_2 layer to metal M_3 with different electrical lengths at 100 GHz. The full schematic of the W-band balanced PA with proposed quadrature coupler is shown in Fig. 9.

D. Simulated S-parameters and Stability Considerations

The simulated small-signal S-parameters are shown in Fig. 12(a). The single-ended three-stage PA owns a simulated S_{21} peak small-signal gain of 22.4 dB at 94 GHz with a 3-dB bandwidth of 89-101 GHz. The simulated S_{11} remains below 10 dB from 92 GHz to 108 GHz, while the S_{22} is below 10 dB from 89 to 92 GHz. In this work, the peak of the small-signal gain of 23.8 dB at 93 GHz with a 3-dB bandwidth of 87-103 GHz is observed in Fig. 12(a). By using the proposed quadrature coupler, the input- and output-reflection coefficients S_{11} and S_{22} of W-band balanced PA are below 10 dB from 81 to 110 GHz, which verifies that the proposed quadrature coupler could enhance the input- and output-matching levels to improve the output power of the PA. Obviously, the simulated isolation S_{12} of both the single-ended and balanced PA are below 50 dB from 80 to 110 GHz. The simulated K-factor and μ-factor for the single-ended and balanced PAs are shown in Figs. 12(b) and (c), respectively. The stability analysis is conducted using ADS showing that the K-factor is >1 and the μ-factor is >0 from DC to 250 GHz, which verifies an unconditional stable characteristic of the proposed structure. While not shown in this study, the balanced PA with proposed coupler owns the higher K-factor and μ-factor than that of single-ended PA. The PAs are unconditionally stable.

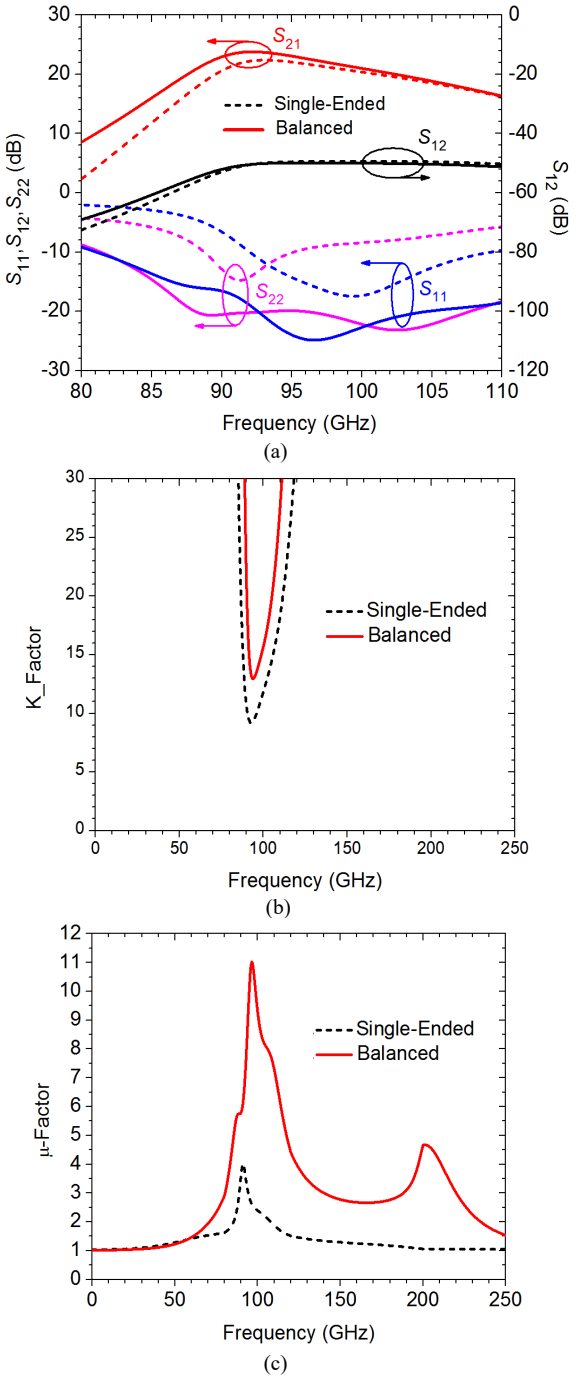

Fig.12. Simulated results of (a) S-parameters (b) K-factor and (c) μ-factor for the single-ended and proposed balanced PA.

IV. MEASUREMENTS

Fig.13 (a) shows the die photograph. The chip area is 0.8×0.8 mm^2 including all pads, while the size of the proposed quadrature coupler using BCSL is 0.2×0.18 mm^2. The W-band PA is measured using an on-chip GSG probe station, a signal generator, a W-band up-conversion and a down-conversion modules, WR-10 waveguides and a spectrum analyzer as shown in Fig.13 (b). In this measurement setup, the W-band up- and down-conversion modules have the fixed output power at about 0 dBm including the power losses of waveguides, GSG probes and cables for interconnections. Due to the limitation of

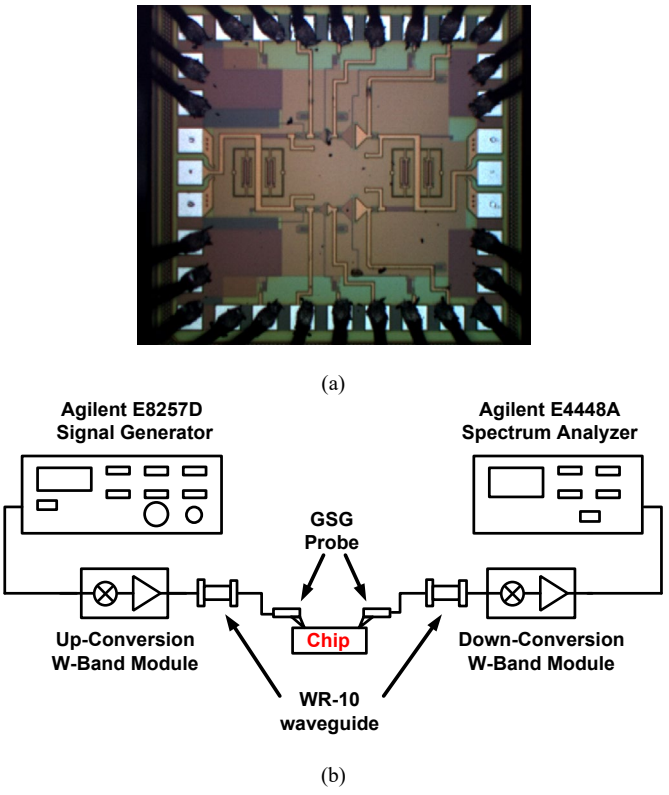

Fig.13. (a) W-band balanced PA with proposed quadrature coupler die photograph in 0.13-μm SiGe. (0.8×0.8 mm^2 including pads) (b) W-band PA measurement setup.

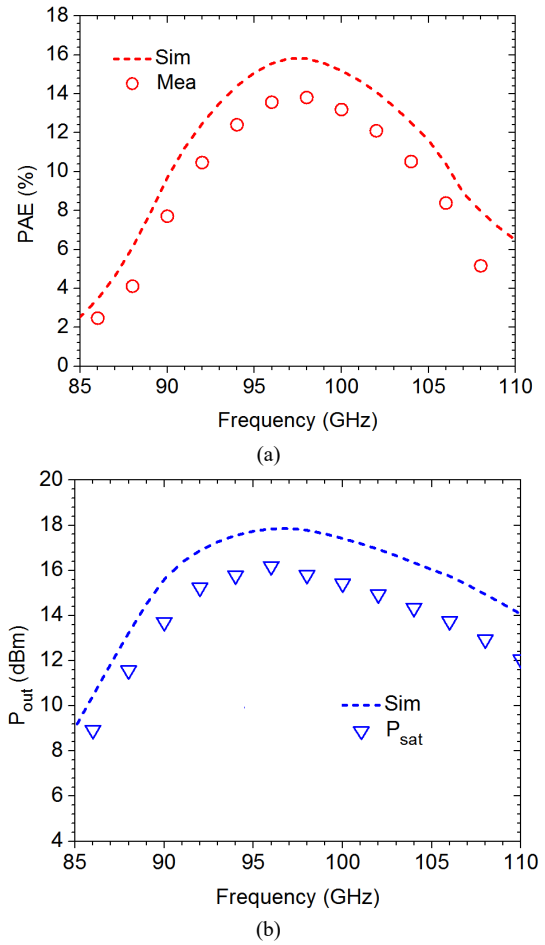

Fig.14. Simulated and measured (a) PAE and (b)P_{sat}, OP_{1dB} versus frequency of balanced PA with proposed quadrature coupler.

the measurement setup as shown in Fig.13 (b), the small-signal S-parameters and the output performances versus input power of the proposed PA could not be obtained and presented. However, we used the fixed input power of 0 dBm (including embedded cable and probe losses) to measure the saturated output power P_{sat} and PAE versus frequency from 80 to 110 GHz. The input W-band signal (80 to 110 GHz) is generated using Agilent E8257D signal generator and up-conversion W-band module. The WR-10 GSG probe loss is approximately 0.6 dB. After the DUT chip, the down-conversion W-band module converts the output signals to the testable frequency range. The Agilent E4448A spectrum analyzer is used to measure the output power of the DUT. Fig. 14 shows the measured PA saturated output power and PAE from 80 to 110 GHz with the same power supply of 2 V. The proposed W-band PA results in a saturated output power of 16.3 dBm at 95 GHz with a peak PAE of 14.1 %. The measured P_{sat} for the W-band PA is >12 dBm at 88-110 GHz with 1-dB bandwidth >9 dBm from 91-102 GHz. Meanwhile, the measured peak PAE is >10% at 92-105 GHz. Table I summaries the measured performances comparing with the reported state-of-the-art W-band PAs.

V.CONCLUSION

A W-band two-way balanced power amplifier (PA) using a compact quadrature coupler with broadside coupled strip-line (BCSL) has been demonstrated in 0.13-μm SiGe HBT. It achieves 16.3 dBm saturated output power with 14.1% PAE at 100 GHz. The proposed W-band balanced PA can be used in beamforming phased array for sub-millimeter high data-rate wireless communications and high-frequency imaging applications.

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TABLE I
COMPARISONS WITH OTHER RELATIVE CIRCUITS.

Ref.	Frequency (GHz)	Technology	Topology	P_{sat} (dBm)	Gain (dB)	Peak PAE (%)	P_{sat}-1dB BW (GHz)	FOM*	V_{dd} (V)	Power Density (mW/ mm^2)	Area** (mm^2)
[16]	94	90nm CMOS	4-stage 4-way comb.	16.8	20	16.4	80-108	88.4	2	39.4	0.69
[17]	90	65nm CMOS	16-way comb.	18.3	12.5	9.5	86-98	79.7	1.2	82.4	0.82
[18]	113	65nm CMOS	3-stage 2-way cascode	13.8	13.4	10	100-117	78.3	2	117	0.21
[19]	86	65nm CMOS	3-stage 2-way comb.	11.9	18.6	9	N/A	78.7	1	41.8	0.37
[20]	110	65nm CMOS	3-stage 2-way comb.	14.8	14.1	9.4	100-110	79.5	2	93.7	0.32
[21]	100	65nm CMOS	4-stage	10	13	7	N/A	71.5	1.2	30.3	0.33
[22]	79	65nm CMOS	4-stage 8-way comb.	19.3	24.2	19.2	77-81	94.3	1	99.5	0.86
[23]	78	180nm SiGe	2-stage 4-way comb.	14	18.3	2	N/A	73.2	3.2	29.6	0.85
[24]	80	130nm SiGe	3-stage 16-way comb.	27.3	19.3	12.4	70-90	95.6	1.8	82.8	6.48
[25]	95	130nm SiGe	quasi-optical 4-stage comb.	22	21.5	5.8	N/A	90.7	N/A	3.3	48
[26]	120	90nm SiGe	4-stage 2-way diff.	17	20	12.5	115-130	89.6	1.6	38.9	1.29
This work	**100**	**130nm SiGe**	**3-stage 2-way balanced**	**16.3**	**14.5**	**14.1%**	**91-102**	**81.8**	**1.6**	**82.3**	**0.64**

* FOM=P_{sat}(dBm)+Gain(dB)+20log10(Freq.(GHz))+10log10(PAE(%))
** Areas include pads.

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