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PLEASE CITE THE PUBLISHED VERSION

<http://dx.doi.org/10.1016/j.vacuum.2017.01.001>

PUBLISHER

Elsevier © The Authors

VERSION

VoR (Version of Record)

PUBLISHER STATEMENT

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Ulicna, Sona, Patrick Isherwood, Piotr M. Kaminski, Michael Walls, Jiaojiao Li, and Colin A. Wolden. 2019. "Development of ZnTe as a Back Contact Material for Thin Film Cadmium Telluride Solar Cells". figshare. <https://hdl.handle.net/2134/24226>.



Development of ZnTe as a back contact material for thin film cadmium telluride solar cells



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ARTICLE INFO

Article history:

Received 21 July 2016

Received in revised form

28 November 2016

Accepted 1 January 2017

Available online 3 January 2017

Keywords:

CdTe solar cells

Thin film

Back contact

Cu-doped ZnTe

Pulsed DC magnetron sputtering

RTP

ABSTRACT

Cadmium telluride (CdTe) is high-efficiency commercialised thin film photovoltaic technology. However, developing a stable low-resistivity back contact to the CdTe solar cells is still an issue. High work function and low level of doping of this material don't allow to create an ohmic contact with metals directly. Copper is commonly used to lower the back contact barrier in CdTe solar cells, but an excessive amount of copper diffusing through the cell is harmful for the device performance and stability. In this work a copper-doped ZnTe (ZnTe:Cu) buffer layer was incorporated in between CdTe and gold metal contact by high-rate pulsed DC magnetron sputtering. The back contact was then activated by rapid thermal processing (RTP) resulting in spectacular improvement in key device performance indicators, open circuit voltage (V_{OC}) and fill factor (FF).

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1. Introduction

Cadmium telluride is one of the leading and most promising materials for thin film solar cells. It has an optical band-gap of around 1.45–1.5 eV which is close to the optimum for photo-conversion, and has a large optical absorption coefficient ($> 10^{-4}/\text{cm}$) [1,2]. It is a direct band-gap semiconductor, with the result that only very thin layers are required to fully absorb photons [1]. CdTe photovoltaic technology currently holds (research) maximum efficiency of 22.1% produced by First Solar [3].

There remain technical difficulties in the construction of CdTe cells however. A key concern, and one of the greatest challenges for CdTe photovoltaic technology is the successful formation of a stable ohmic back contact [4]. The large electron affinity ($\chi = 4.5$ eV) and low carrier density of the CdTe absorber contribute to the formation of a back contact Schottky barrier, which acts diode set up in opposition to the CdS/CdTe junction [5,6]. This barrier limits hole collection at the back contact, causes losses in open circuit voltage (V_{OC}) and fill factor (FF) and can be observed through the occurrence of roll-over (current-limiting inflection point) in J-V curves [6,7]. To form an ohmic contact on p-type CdTe, a metal with a work

function > 5.9 eV (sum of CdTe band-gap and electron affinity) is needed. As such metals are not available, the formation of Schottky barrier is inevitable [8].

To overcome this problem, one potential solution is to insert a thin interfacial buffer layer between the metal contact and the CdTe absorber. A material of increasing interest for this buffer layer is copper doped zinc telluride (ZnTe:Cu), with a copper doping level of between 1 and 5 wt% [4]. ZnTe was chosen because of its chemical stability and the near-perfect alignment of the CdTe and ZnTe valence bands, enabling facile hole transport [9]. The potential for high acceptor level doping of ZnTe ($> 10^{20}/\text{cm}^3$) could also allow for formation of an effective tunnel junction to the metal layer [10]. Copper is one of the most frequently used materials for enhancing CdTe device performance [11]. Cu concentration contributes to the creation of an ideal back contact through increasing the carrier concentration, thereby decreasing the potential barrier. This results in increased saturation current [12]. Copper is however a mobile element and is prone to diffuse away from the back contact and further into the cell. Excessive copper doping can lead to device degradation through reduced carrier lifetime as well as deep level defects in the CdTe bulk which cause increased recombination and consequently reduced short circuit current (J_{SC}) and V_{OC} [11]. Further long-term instability is caused by copper diffusion into the CdS window layer where reduction in net donor density ($N_D - N_A$)

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has been observed [13]. It is therefore clear that even though ZnTe:Cu is thought to form a low resistance contact, careful control of the Cu to prevent it diffusing away from the back contact and into the bulk CdTe and CdS is critical [14]. In this work ZnTe:Cu layers were deposited by high rate pulsed-DC magnetron sputtering. Diffusion of copper into the device is greatly enhanced through sustained and elevated temperatures, making it difficult to control [12]. Whilst deposition of ZnTe:Cu at elevated temperatures would have significant advantages in terms of crystal growth and effective incorporation of the layer into the cell, separation of the deposition and heating stages would allow for dramatically reduced heating times and hence a reduced risk of copper diffusion. Separation of the two can theoretically be achieved through deposition of ZnTe:Cu and the metal back contact layer at room temperature followed by either a simple thermal treatment in a furnace or rapid thermal processing (RTP) [4].

2. Experimental details

2.1. ZnTe deposition on glass

ZnTe:Cu films were deposited onto ultrasonically cleaned soda lime glass substrates using an AJA International Orion 8 HV sputter coater equipped with an Advanced Energy Pinnacle Plus pulsed DC power supply. Deposition took place at 1mTorr (0.133 Pa) under argon, with an argon flow rate of 7 standard cubic centimetres per minute (SCCM). Power was maintained at 105 W, with a frequency of 220 kHz and a reverse time of 2 μ s. Depositions were run at room temperature, and films were deposited from a single predoped ceramic target. Deposition time was varied so as to obtain an accurate deposition rate, with time steps of 900, 1800, 2700 and 3600s. A second set of samples was obtained through variation of power pulsing frequency, using frequencies of 150, 180, 200 and 220 kHz.

Film thickness was measured using an Ambios XP-2 stylus profilometer. X-ray diffraction (XRD) was carried out using a Bruker D2 Phaser X-ray diffractometer equipped with a Lynxeye™ detector and Cu-K α X-ray source. Measurements were taken at 2 θ angles of 20°–90°. The obtained patterns were compared to those from the International Centre for Diffraction Data crystallographic database [15]. Film sheet resistance was determined at several locations on each film using a four-point probe.

2.2. Device fabrication

Preformed superstrate-configuration CdTe devices were provided by Colorado State University (CSU). The CSU deposition process involves deposition of an intrinsic tin oxide layer followed by reactively sputtered oxygen-doped CdS and close-space sublimation of CdTe. The substrate is Corning 7059 glass with a fluorine-doped tin oxide TCO layer [16]. The completed stack undergoes a standard thermochemical treatment with cadmium chloride (CdCl₂). These devices were then coated with a 300 nm thick ZnTe:Cu buffer layer at room temperature using the same conditions as described above, with a power pulsing frequency of 220 kHz and 2 μ s reverse time. Devices of an area of 0.25 cm² were defined by sputtering a 100 nm thick gold contact using a shadow mask in a Quorum Q150T mini sputter coater. Individual cells were electrically isolated by scribing. Fully contacted devices deposited at room temperature were subjected to thermal treatments to activate the back contact. This was carried out by Colorado School of Mines (CSM) in a rapid thermal processing (RTP) furnace. Since the optimum process temperature varies with different architectures, initial RTP temperature was kept relatively low and was then raised progressively until the optimum temperature was found. The

devices were placed on an aluminium nitride (AlN) susceptor in the RTP furnace and received consecutive annealing steps starting at 260 °C and ending at 400 °C under flowing Ar. Temperature was measured using a K-type thermocouple in contact with the AlN susceptor. Each step consisted of a rapid (10s) ramp to the desired setpoint and a 30s dwell-time. The lamps were then turned off and the sample allowed to cool to room temperature naturally. Once the optimum setpoint had been determined, a second sample was treated at this temperature.

The electrical performance of CdTe device was measured before and after successive RTP treatments under simulated AM1.5 g light using a commercial solar simulator which was calibrated using a certified standard silicon cell [17]. 5 to 7 individual devices were measured each time.

Transmission electron microscopy (TEM) was used to investigate cell microstructure. High resolution TEM cross sections were obtained using an FEI Technai F20 field emission gun transmission electron microscope. The TEM samples were prepared by a standard in-situ lift out method using a dual beam FEI Nova 600 Nanolab scanning electron microscope [16].

3. Results and discussion

3.1. Process and material characterisation

ZnTe:Cu film thickness was found to be proportional to sputter time, with an observed deposition rate of 0.33 nm/s at 220 kHz (Fig. 1). As a result, a 300 nm thick ZnTe:Cu layer was grown in only 15 min. The deposition rate can be further increased either through increasing the amount of power applied to the pulsed-DC gun or through decreased pulse frequency. Pulse frequency was shown to have a small and non-linear impact on deposition rate (Fig. 2).

The bright field TEM image of the full CdTe device with as-deposited ZnTe:Cu layer is shown in Fig. 3 and Fig. 4 shows the detailed view of the back contact region. All the thin film layers are well defined. Nanostructured ZnTe:Cu layer is uniformly deposited on the top of the CdTe grains.

The XRD patterns of 300 nm thick ZnTe:Cu film sputtered on glass substrates and annealed at different RTP process temperatures are plotted in Fig. 5. Peak positions were identified using the International Centre for Diffraction Data (ICDD) crystallography database [15]. The three most pronounced peaks were found to be

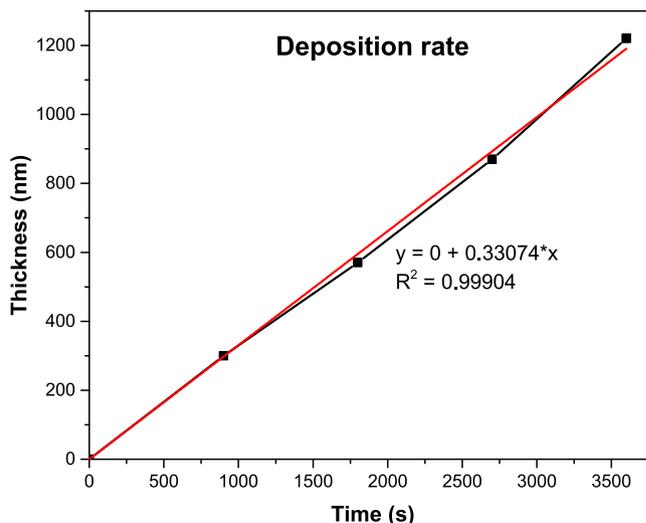


Fig. 1. Deposition rate of ZnTe:Cu film sputtered on glass using pulsed-DC magnetron sputtering at 220 kHz, 2.0 μ s, 105 W.

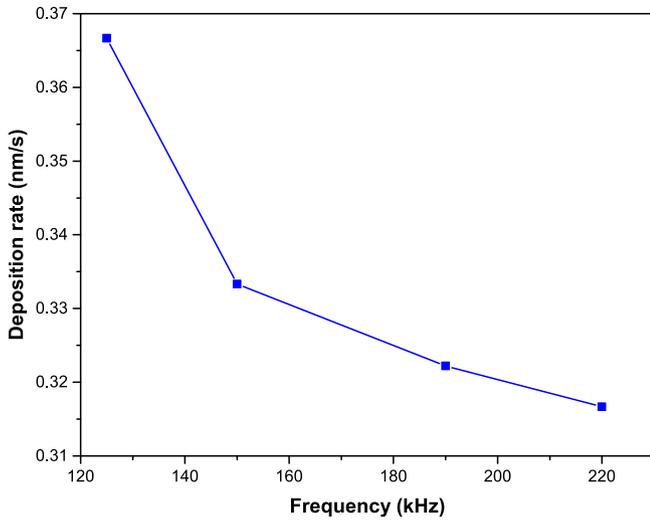


Fig. 2. Deposition rate as a function of frequency of power supply pulses.

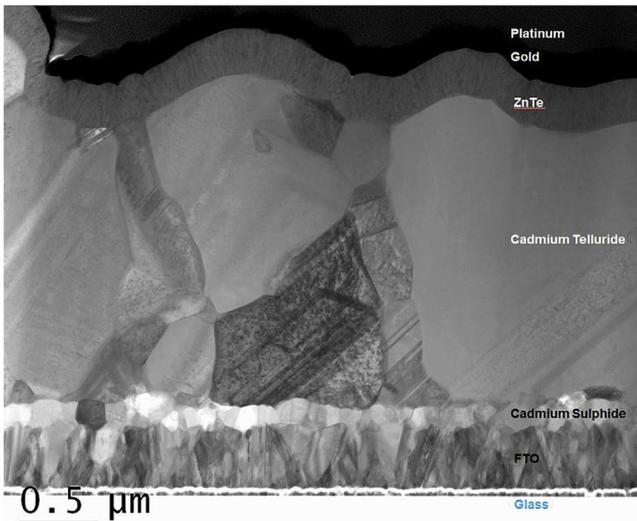


Fig. 3. Bright field TEM image of the full CdTe solar cell incorporating as-deposited pulsed DC magnetron sputtered ZnTe:Cu back contact interface layer.

at 2θ angles of 25.18° , 41.63° and 49.15° , and correspond to the (111), (220) and (311) planes of cubic ZnTe respectively. The peak size increased when the as-deposited film was annealed at sufficiently high temperature, forming better crystallised films. The 260°C RTP treatment resulted in very similar XRD properties to the as-deposited film. An additional peak was formed at a 2θ angle of 27.50° when 380°C and 400°C RTP processes were employed. This peak does not appear to correspond to any ZnTe phases, but perhaps Cu_xTe clusters ($1 < x < 2$) that were found in previous work in RTP annealed CdTe cells with co-evaporated ZnTe:Cu buffer layer [16]. Measurements of sheet resistance were off-scale for the as-deposited and annealed at 260°C samples, but the sheet resistance was successfully measured for the 380°C and 400°C RTP processed films. It was found to be $5.5\text{ k}\Omega/\text{sq}$ and $3.8\text{ k}\Omega/\text{sq}$ respectively. Deriving from these results, the film resistivity decreased with the increase of RTP temperature while the crystallinity of the film improved. Paradoxically, even a high resistivity ZnTe:Cu film deposited by pulsed DC magnetron sputtering can form a low-resistivity quasi-ohmic back contact for CdTe devices.

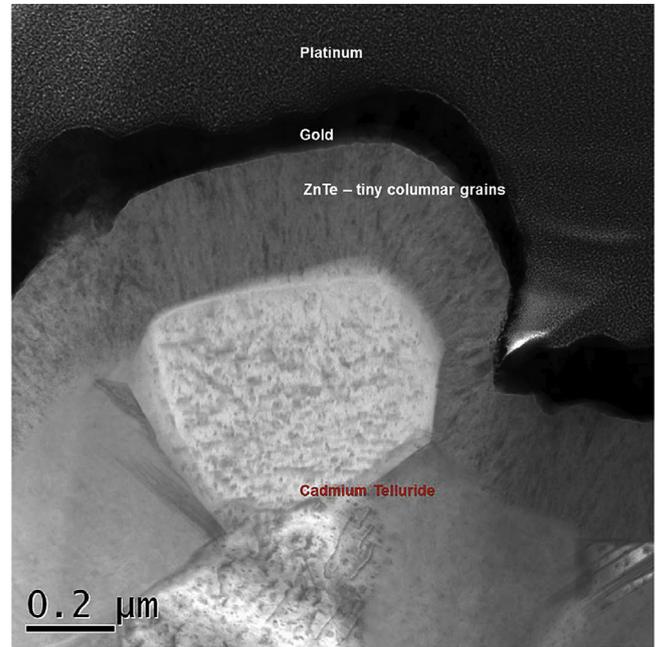


Fig. 4. Cross-sectional TEM image of the as-deposited ZnTe:Cu layer.

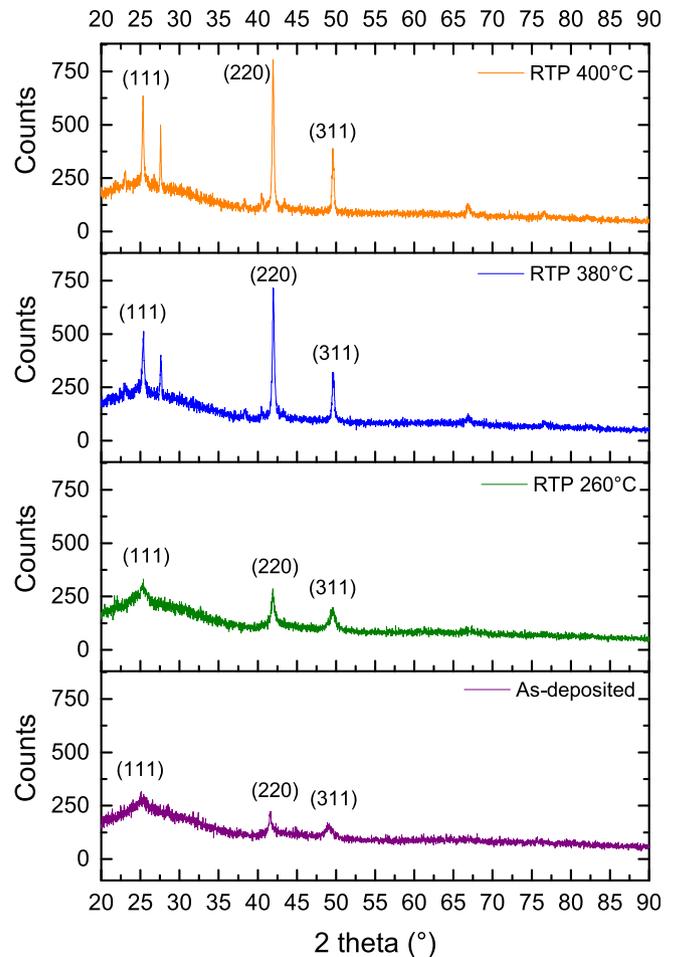


Fig. 5. X-ray diffraction patterns of ZnTe:Cu films sputtered on glass and annealed with RTP.

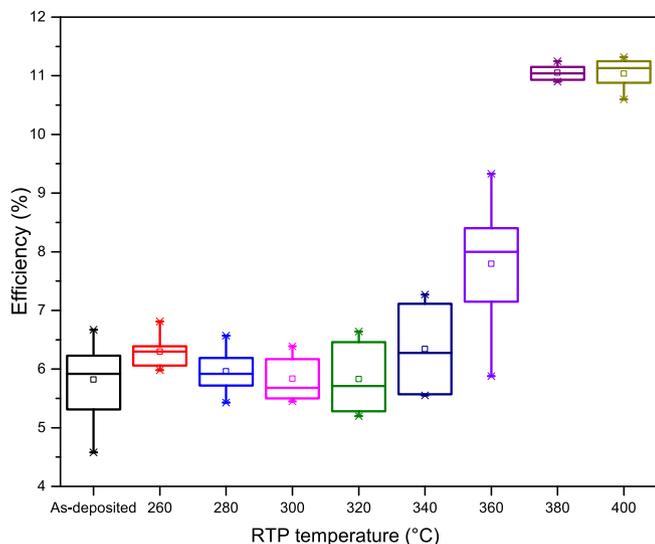


Fig. 6. RTP temperature optimisation.

3.2. Device fabrication and characterisation

To optimise the RTP process, a number of subsequent treatments were performed at progressively higher temperatures starting at 260 °C, increasing in 20 °C increments and finishing at 400 °C after device performance started to degrade. RTP treatment resulted in increased efficiency compared to as-deposited devices, and the optimum temperature was found to be 380 °C (Fig. 6). A second sample was exposed to a refined RTP treatment, whereby the temperature was increased in 10 °C increments around the optimum found previously. The devices exposed to treatment at 380–390 °C exhibited the best efficiency. This value is slightly higher than that found in the literature for a co-evaporated ZnTe:Cu layer (320–330 °C) [17].

Fig. 7 compares J-V curves of devices in the as-deposited state, after an optimal RTP treatment (380 °C) and from an under- and an overheated sample (360 °C and 400 °C respectively). Their main performance indicators are summarised in Table 1. All devices show similar carrier collection, with the main improvement coming from the increase in V_{OC} and FF. After the optimum RTP treatment, V_{OC}

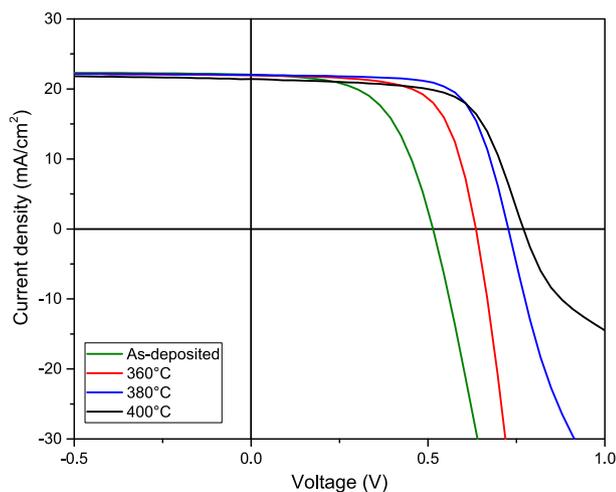


Fig. 7. J-V curve of four representative devices exposed to different RTP temperature treatments.

Table 1

Main performance indicators of devices from Fig. 7.

RTP process	V_{OC} (V)	J_{sc} (mA/cm ²)	Fill Factor (%)	Efficiency (%)
As-deposited	0.5142	22.039	56.83	6.44
360 °C	0.6357	21.956	66.81	9.33
380 °C	0.7273	21.99	70.32	11.25
400 °C	0.7698	21.408	66.04	10.88

increased by more than 200 mV, reaching 727.3 mV, and FF by more than 13%, up to 70.32%. This is consistent with the elimination of the barriers at the back contact. The overall efficiency increased from 6.44% to 11.25%. At slightly higher than optimum RTP temperature, the FF started to decrease and a roll-over appears on the J-V curve. The current starts to decrease slightly, which can be attributed to the excess of copper migrating towards the CdTe/CdS junction and creating recombination centres and causing shunting. This needs to be proven by further investigation of copper behavior after RTP of CdTe solar cells containing sputtered ZnTe:Cu interface layer. In order to explain the device performance, an attempt was made to measure the carrier density using capacitance-voltage (CV) technique. These measurements gave unreliable and unrepeatable results however, rendering them unusable. CV measurement of CdTe solar cells is often complicated by the presence of deep level defects, back contact barriers, finite absorber thickness and non-uniform carrier density. All of these can contribute to erroneous carrier density readings [18].

4. Conclusions

This study demonstrates that inclusion of a ZnTe:Cu buffer layer at the back contact of CdS/CdTe solar cells improves device performance, dramatically increasing both V_{OC} and FF. The ZnTe:Cu layer was successfully deposited by high rate pulsed-DC magnetron sputtering giving devices which performed well overall. The rapidity of the process could give a substantial time and money saving in CdTe manufacturing. Device performance is however sensitive to post-deposition annealing temperature. Highly effective and versatile RTP separates the deposition and activation of the ZnTe:Cu layer and perhaps reduces Cu migration into the CdTe absorber, which could be a step towards the improvement of the device stability.

Acknowledgements

The authors would like to acknowledge RCUK for providing financial support through the SuperGen SuperSolar Hub (EPSRC Grant No. EP/J017361/1).

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