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# Compact and Low-Power Under-Voltage Lockout and Thermal-Shutdown Protection Circuits Using a Novel Low- $I_Q$ All-in-One Bandgap Comparator

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**Abstract**—This paper presents a novel and compact bandgap comparator (BGRCOMP) for under-voltage lockout (UVLO) and thermal shutdown (TSD) protection circuits. The proposed BGRCOMP is self-referenced and combines the advantages of both a high-accuracy bandgap reference and a comparator into one single circuit. A latch-controlled biasing technique is also presented, which reduces static power consumption of the proposed BGRCOMP. The proposed BGRCOMP is used for the design of compact and low power UVLO and TSD circuits. The post-layout simulation results using a 0.18  $\mu\text{m}$  BCD-on-SOI technology prove the attractive performance of the UVLO and TSD with a static current ( $I_Q$ ) of 7.76  $\mu\text{A}$  and 5.4  $\mu\text{A}$  from a 5 V supply, respectively. The deviations of UVLO thresholds are less than 3 mV in the temperature range of  $-40$ – $85$   $^\circ\text{C}$ .

**Keywords**—Bandgap comparator (BGRCOMP), under-voltage lock-out (UVLO), thermal shutdown (TSD), low power, protection circuits.

## I. INTRODUCTION

Nowadays, electronic systems integrate various functions on the same die to achieve compactness, improve performance and reduce cost. To enhance the reliability requirement of these systems, under-voltage lockout (UVLO) and thermal shutdown (TSD) circuits are frequently needed for most integrated circuit (IC) systems as shown in Fig. 1(a) [1-2]. The UVLO circuit is employed to prevent the operation of circuits in case of a supply voltage failure. The TSD circuit senses and detects high temperature within the IC to turn off the source of heat when the temperature is higher than a certain preset value.

Fig. 1(b) shows conventional UVLO and TSD circuits consisting of three basic blocks: a sensor, a voltage reference and a hysteresis comparator. The temperature sensor of the TSD senses the temperature within the IC and converts the temperature into temperature-dependent voltage,  $V_s(T)$ .  $V_s(T)$  is then compared with a voltage reference  $V_{REF}$  to detect the critical temperature condition and output a TSD signal. In the same way, the voltage sensor in the UVLO senses the value of the bias supply VDD and compares this sensing value  $V_s(V)$  with  $V_{REF}$  to detect the under-voltage condition and output a UVLO signal. These conventional UVLO and TSD structures have been widely applied and reported in the literature [3-10]. However, several issues related to the design of UVLO/TSD circuits remain. First, a dedicated  $V_{REF}$  is needed, so the power consumption is high as in the UVLO designs reported by Song [3], Cho [4], and the design of the TSD reported by Ding [8]. A second very important issue for the design of TSD and UVLO is reducing the static quiescent current of the utilized

comparator, especially for the applications where the power supply is limited. The reason for this is that except UVLO/TSD circuits continue to operate when UVLO, TSD conditions occur, the other blocks of the IC are off. A third issue is that the accuracy of the trip points (voltage thresholds of UVLO and temperature threshold of TSD) for the UVLO and TSD circuits is low [3,5,7]. In order to simplify the design and reduce power consumption, a non-bandgap structure has been proposed [11]. However, the drifts of the trip points are even worse and not well defined. Therefore, the design of low power UVLO/TSD with precise trip points remains a challenge.

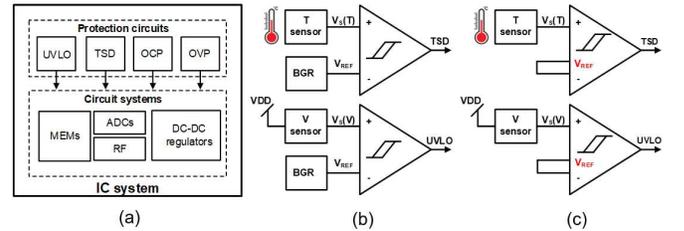


Fig. 1. (a) IC system with the integration protection functions, (b) Conventional structures and (c) new structure of the UVLO and TSD.

This paper proposes new solutions for the design of low-power, size-compact UVLO and TSD using a novel bandgap comparator as shown in Fig. 1(c). In this structure, a dedicated bandgap  $V_{REF}$  is no longer needed since the proposed bandgap comparator (BGRCOMP) can work as a comparator and provide a high-precision internal reference voltage. The two main contributions of this paper are: (1) a novel BGRCOMP with low quiescent current and (2) new UVLO and TSD circuits using the proposed BGRCOMP.

The rest of the paper is organized as follows: Section II presents the proposed BGRCOMP circuit. In Section III, the application of BGRCOMP in designing UVLO and TSD circuits is presented. Section IV provides circuit design and post-layout simulation results of the UVLO and TSD. Finally, Section V draws the main conclusions of this works.

## II. PROPOSED BANDGAP COMPARATOR

The proposed BGRCOMP in Fig. 2 consists of 4 stages. The first stage includes Q1, Q2, R1, R2 and a latch load MP1-MP4 that constitutes the core of the BGRCOMP. Q1, Q2, R1, and R2 compose the comparator utilizing the bandgap reference principle, so an internal reference voltage exists. The second stage (MN1-MN2, MP5-MP6) with an amplification current factor of M is used to increase the gain and the resolution of the comparator. Two latches (MN3-MN8, MP7-

MP12) help to provide a rail-to-rail output. The two extra switches  $M_{SW1}$  and  $M_{SW2}$  help to reduce quiescent current.

### 2.1 Bandgap comparator operation principle

Fig. 3(a) shows the core of the proposed BGRCOMP. As will be explained below, this structure can self-generate an internal reference and compare the input voltage with this internal reference value. For the ease of analysis, assume that Q1 and Q2 are in the forward-active region. As the emitter area of Q2 is  $N$  times that of Q1,  $I_{S2} = N \times I_{S1}$  where  $I_{S1}$  and  $I_{S2}$  are the saturation currents of Q1 and Q2, respectively. The large-signal collector currents of Q1 and Q2 can be expressed as:

$$i_{C1} = I_{S1} \times e^{\frac{v_{IN} - (i_{C1} + i_{C2})R_2}{U_T}}; \quad i_{C2} = N \times I_{S1} \times e^{\frac{v_{IN} - (i_{C1} + i_{C2})R_2 - i_{C2}R_1}{U_T}} \quad (1)$$

where  $U_T = kT/q$  is the thermal voltage,  $q$  is the electronic charge,  $k$  is the Boltzmann constant, and  $T$  is the temperature. The current ratio between  $i_{C1}$  and  $i_{C2}$  can be formulated as:

$$\frac{i_{C1}}{i_{C2}} = \frac{1}{N} \times e^{\frac{R_1 i_{C2}}{U_T}} \quad (2)$$

We define a balancing condition at which  $i_{C1} = i_{C2} = i_{CB}$  and  $v_{IN} = V_{INREF}$  where  $i_{CB}$  and  $V_{INREF}$  can be expressed as:

$$\frac{i_{C1}}{i_{C2}} = \frac{1}{N} \times e^{\frac{R_1 i_{CB}}{U_T}} = 1; \quad i_{C1} = i_{C2} = i_{CB} = \frac{1}{R_1} \times \frac{kT}{q} \ln(N) \quad (3)$$

$$V_{INREF} = V_{BE1} + 2 \times \frac{R_2}{R_1} \frac{kT}{q} \ln(N) \quad (4)$$

Fundamentally,  $V_{INREF}$  in (4) is a function of temperature. It is well known that the  $V_{BE1}$  is complementary to absolute temperature (CTAT) while  $kT/q$  is proportional to absolute temperature (PTAT). With proper values of design parameters  $R_1$ ,  $R_2$ ,  $N$ ,  $V_{INREF}$  can be designed to be insensitive w.r.t temperature variations. Under this balancing condition, as  $i_{C1} = i_{C2}$ ,  $V_A = V_B$ .

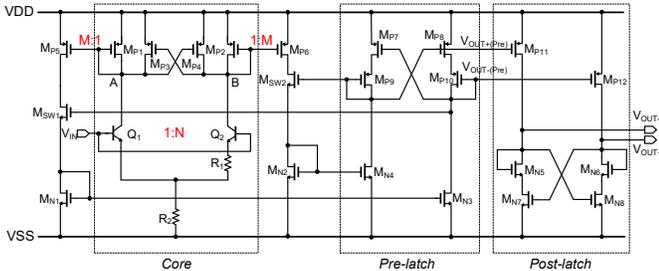


Fig. 2. The proposed bandgap comparator consisting of internal reference voltage and latch-based control for low  $I_Q$ .

From (1), it can be seen that  $i_{C1}$  and  $i_{C2}$  are functions of  $v_{IN}$ . When  $v_{IN} \neq V_{INREF}$ :  $i_{C1} \neq i_{C2}$ , the BGRCOMP is out of the balancing condition. According to the value of  $v_{IN}$ , there are two scenarios depicted in Fig. 3(b) as follows:

- When  $v_{IN} < V_{INREF}$ , both of  $i_{C1}$  and  $i_{C2}$  are lower than  $i_{CB}$ . As  $i_{C2} < i_{CB}$ , from (2) and (3) it can be verified that  $i_{C1}/i_{C2} < 1$ , i.e.  $i_{C1} < i_{C2}$ . The current difference between  $i_{C1}$  and  $i_{C2}$  triggers the latch load  $M_{P1}$ - $M_{P4}$ . Voltage  $V_B$  at node B is pushed down and  $V_A$  at node A is pulled up to VDD.
- When  $v_{IN} > V_{INREF}$ , both of  $i_{C1}$  and  $i_{C2}$  are higher than  $i_{CB}$ . As  $i_{C2} > i_{CB}$ , from (2) and (3) it can be verified that  $i_{C1}/i_{C2} > 1$ ,

i.e.  $i_{C1} > i_{C2}$ . The current difference between  $i_{C1}$  and  $i_{C2}$  triggers the latch load. This current difference triggers the latch load  $M_{P1}$ - $M_{P4}$ . Voltage  $V_B$  at node B is pulled up to VDD and  $V_A$  is pushed down.

Through the above analysis, when the value of  $v_{IN} = V_{INREF}$ , the comparator is in balancing state and helps to define an internal temperature-insensitive reference voltage. The operation of the bandgap comparator can now be modeled as a comparator with its internal bandgap reference as shown in Fig. 1(c) in which the input voltage  $v_{IN}$  to its internal temperature-insensitive voltage reference  $V_{INREF}$ .

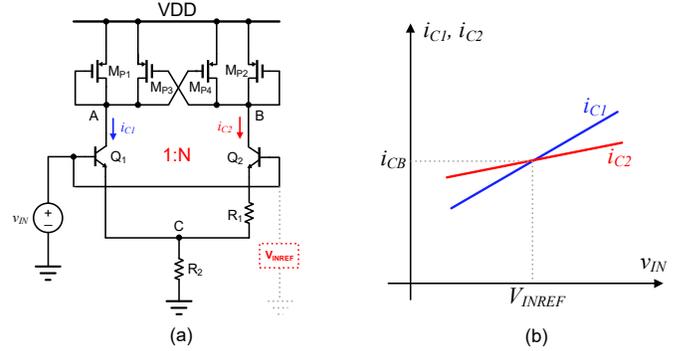


Fig. 3. (a) Core of the bandgap comparator. (b) Variations of the collector currents  $i_{C1}$  and  $i_{C2}$  versus  $v_{IN}$ .

It should be noted that the proposed BGRCOMP in Fig. 2 utilizes BJT devices that might not be available with the standard CMOS process [12-13]. Another low-cost technique and highly compatible for digital CMOS technologies is to use a MOSFET pair in sub-threshold (weak inversion) replacing the Q1-Q2 pair. In sub-threshold regime, when the gate-source voltage is lower than the threshold voltage ( $V_{GS} < V_T$ ), MOSFET works as a lateral BJT device [14-15].

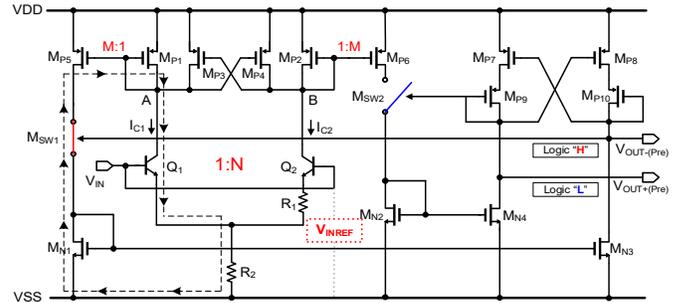


Fig. 4.  $I_Q$  reduction with latch-controlled technique [16].

### 2.2 Low- $I_Q$ BGRCOMP with latch-controlled method

To reduce power consumption, a latch-controlled biasing technique is also implemented with switches  $M_{SW1}$  and  $M_{SW2}$  that are controlled by the pre-latch ( $M_{N3}$ - $M_{N4}$ ,  $M_{P7}$ - $M_{P10}$ ) [16]. Fig. 4 shows the operation of the comparator (without the pre-latch for the sake of simplicity) for the pre-latch state:  $V_{OUT(-)Pre} = \text{HIGH}$ ,  $V_{OUT(+Pre)} = \text{LOW}$ . When  $v_{IN} > V_{INREF}$ ,  $i_{C1} > i_{C2}$  and the latch load ( $M_{P1}$ - $M_{P4}$ ) is triggered so that the drain current through  $M_{P1}$  increases rapidly and the drain current of  $M_{P2}$  decreases rapidly to zero. The generated current through  $M_{P1}$  is copied and amplified ( $\times M$ ) by the current mirrors  $M_{P1}$ - $M_{P5}$ / $M_{N1}$ - $M_{N3}$  and pulls  $V_{OUT(-)Pre}$  from HIGH to LOW.

Therefore, the pre-latch flips its internal states. When  $V_{IN} < V_{INREF}$ , the current through MP1 decreases to zero while the current through MP2 increases rapidly. However, since the output state of the pre-latch keeps  $M_{SW2}$  off, the triggering current from the current mirror MP2-MP6 cannot be copied to MN2-MN4. In this case, the internal logic of the pre-latch holds. The operation of the comparator using latch-controlled technique for the pre-latch state  $V_{OUT(-)(Pre)} = \text{LOW}$ ,  $V_{OUT(+)(Pre)} = \text{HIGH}$  is similar.

As a result of the latch-controlled biasing technique, the triggering currents  $M \times I_{MP1}$  and  $M \times I_{MP2}$  are generated only when the pre-latch changes its output state, i.e. the static current of the overall BGRCOMP is only in the first stage. This helps to minimize the quiescent current ( $I_Q$ ) of the proposed BGRCOMP. Besides, by using a high value of  $R_1$  and  $R_2$ ,  $I_Q$  could be designed in a nA range.

### III. DESIGN OF UVLO AND TSD PROTECTION CIRCUITS

#### 3.1 Design of BGRCOMP-based Under-Voltage Lockout

Fig. 5(a) shows the proposed UVLO, which is composed of the proposed BGRCOMP and a voltage sensor that is simply a voltage divider network ( $R_1, R_2, R_H$ ). The voltage sensor  $R_1$ - $R_H$  senses the VDD values  $V_S(\text{VDD})$  and compares the internal  $V_{INREF}$  of the BGRCOMP. The output of the comparator is under-voltage signal (UVLO), depending on the relative value between the  $V_S$  and  $V_{INREF}$ . The operation of the proposed UVLO can be briefly summarized as following: when VDD is low,  $V_S < V_{INREF}$ , meaning that the system supply VDD is in under-voltage state, the BGRCOMP compares  $V_S$  and  $V_{INREF}$  and outputs a signal at low logic (UVLO = '0'). When VDD increases, meaning that the system supply VDD is in a safe range,  $V_S$  increases and surpasses  $V_{INREF}$  of the BGRCOMP, the BGRCOMP outputs a signal at high logic (UVLO = '1'). The UVLO output signal of the UVLO is then used to allow the ON/OFF operation of the IC as shown in Fig. 1(a). To avoid an output oscillation when  $V_S$  fluctuates around  $V_{INREF}$ , a hysteresis is added and controlled by the switch  $SW_{HYS}$  which bypasses  $R_H$ . As the on-resistance of  $SW_{HYS}$  is small to bypass  $R_H$ , the size of  $SW_{HYS}$  is large; therefore,  $SW_{HYS}$  is driven by a buffer that consists of 2 inverters connected in series.

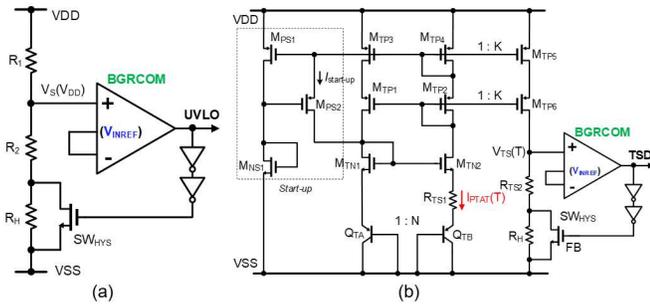


Fig. 5. Schematic of: (a) BGRCOMP-based UVLO, (b) BGR-based TSD.

#### 3.2 Design of BGRCOMP-based Thermal Shut-Down

A simplified schematic of the proposed TSD circuit is constructed using a BGRCOMP, a PTAT temperature sensor, a start-up circuit, and a switch  $SW_{HYS}$  driven by buffers BUFF (Fig. 5(b)). The temperature sensor circuit generates a voltage-

dependent  $V_{TS}(T)$ , which is then compared to the internal reference  $V_{INREF}$  of the BGRCOMP. The PTAT temperature sensor is the current mirror BGR. Compared to PTAT temperature sensor based on [8], there is no need for the use of an op-amp, thus making area and power consumption lower. As the current mirror temperature sensor is self-biased, the startup circuit is included to avoid them from off state.

For the current mirror temperature sensor, the emitter areas of  $Q_{TA}$  and  $Q_{TB}$  are set as 1:N. By setting up the same size ratio for the current mirror MNT1-MNT2 and MPT1-MPT4, the collector currents of  $Q_{TA}$  and  $Q_{TB}$  are equal and the following relationship can be derived:

$$V_{TS}(T) = K \times I_{PTAT}(T) \times R_{TS2} = K \times \frac{R_{TS2}}{R_{ST}} \times \frac{kT}{q} \ln(N) \quad (4)$$

The  $V_{TS}(T)$  is proportional to the absolute temperature  $T$  and depends on the design parameters  $K$ ,  $R_{TS1}$ ,  $R_{TS2}$ ,  $N$  and physical constants  $k$ ,  $T$ ,  $q$ . In particular,  $V_{TS}(T)$  depends on the relative ratio of  $R_{TS1}$  and  $R_{TS2}$ , not their absolute values; thus, the  $V_{TS}(T)$  tracks the temperature  $T$  with a very high accuracy despite process variation. By letting  $V_{TS}(T) = V_{INREF}$ , the preset critical temperature  $T = T_{CRIT}$  can be found. The operation of the proposed BGRCOMP based TSD can be briefly summarized as follows: when the temperature  $T$  is low,  $V_{TS}(T)$  is lower than  $V_{INREF}$  of the BGR comparator, thus making the output of the TSD at low logic (TSD = '0'), meaning that the IC's temperature is low and in a safe range for the IC's operation. When the temperature increase,  $V_{TS}(T)$  increases and surpasses  $V_{INREF}$  of the BGRCOMP, the BGRCOMP outputs a signal at high logic (TSD = '1'), meaning that the IC's temperature is higher than a safe level. The TSD output signal of the TSD circuit is then used to allow the ON/OFF operation of the IC as shown in Fig. 1(a).

### IV. CIRCUIT DESIGN AND POST-LAYOUT SIMULATIONS

#### 4.1 UVLO and TSD design specifications

The proposed UVLO/TSD circuits based on BGRCOMP are targeted for the use in the design of gate drivers, such as in [17-18]. The trip-point specifications of the UVLO and TSD circuits are set at 4.4 V/4.2 V (hysteresis window  $\Delta V_{TH} = 200$  mV) and 90°C/70°C (hysteresis window  $\Delta T = 20^\circ\text{C}$ ), respectively.

#### 4.2 Layout and post-layout simulation results

The proposed BGRCOMP, UVLO and TSD circuits have been designed and simulated in a 0.18  $\mu\text{m}$  BCD-on-SOI process with VDD = 5 V. For the BGRCOMP, the key design parameters were calculated and tuned as follows:  $Q_1 = 3 \mu\text{m}/2 \mu\text{m}$ ,  $N = 4$ . The balancing condition of  $I_{C1} = I_{C2} = 448$  nA was selected which is determined by the value of biasing resistor  $R_1 = 78$  k $\Omega$ ,  $R_2 = 8 \times 78$  k $\Omega$ . Figure 6(a) shows the testbench to determine the  $V_{INREF}$  of the BGRCOMP and Fig. 6(b) shows the pre-layout simulation results. These results show that the BGRCOMP has a very small internal reference variation of 240  $\mu\text{V}$  (2.68 ppm/ $^\circ\text{C}$ ) over a temperature range of  $-40^\circ\text{C}$  to  $100^\circ\text{C}$ , thanks to the high amplification factor ( $\beta$ ) of the utilized BJTs and temperature coefficient of the resistors  $R_1$ ,  $R_2$ . Figure 6(c) shows the propagation delay of the

BGRCOMP at different input voltage ( $V_{IN} - V_{INREF}$ ) to verify that the BJT BGRCOMP is fast enough for UVLO and TSD designs with a delay lower than 1  $\mu$ s.

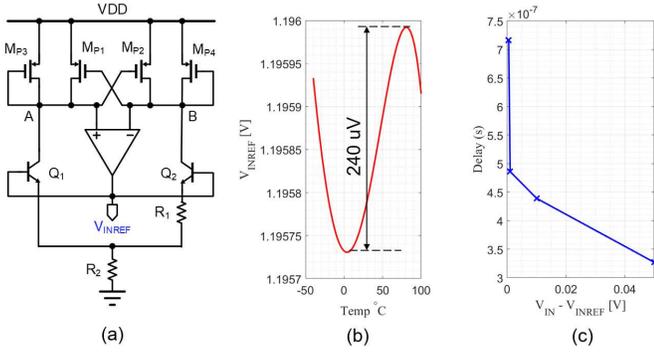


Fig. 6. (a) Testbench to determine  $V_{INREF}$  of the BGRCOMP, (b) Pre-simulation results of  $V_{INREF}$ , (c) Pre-layout delay the BGRCOMP.

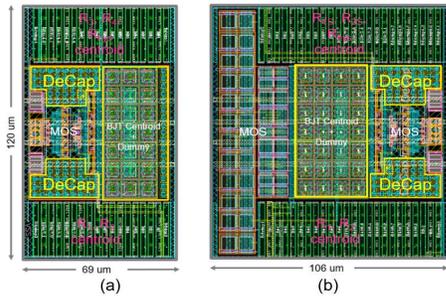


Fig. 7. Layouts of the proposed BGRCOMP-based (a) UVLO and (b) TSD.

Figure 7 shows the layout of the proposed BGRCOMP based UVLO and TSD circuits. The active area is 0.0083 mm<sup>2</sup> (120  $\mu$ m $\times$ 69  $\mu$ m) for the UVLO and 0.0127 mm<sup>2</sup> (120 $\mu$ m $\times$ 106 $\mu$ m) for the TSD. The main area for the UVLO layout is for the resistors and BJTs. If the dummy devices and decoupling capacitors (DeCap) are not included, the chip area can be reduced further. To achieve good performance, systematic mismatch errors were reduced by using several layout techniques such as common centroid and symmetry for input differential BJT pair, latch load, current mirror, resistive divider in the design of UVLO and TSD. The layouts were extracted and simulated with Spectre simulator.

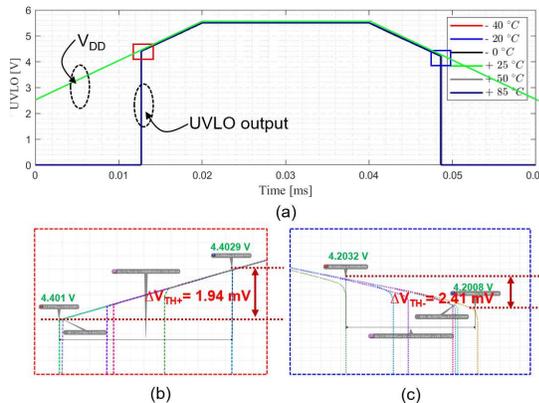


Fig. 8. UVLO post-layout simulation results at different temperatures.

Figures 8 and 9 show the post-layout simulation results for the UVLO and TSD, respectively. The VDD is swept between

0 to 5 V to observe the output of the UVLO. The high and low thresholds are 4.4 V and 4.2 V, respectively, as expected (Fig. 8(a)). Thanks to the temperature-insensitive internal reference voltage  $V_{INREF}$  of the BGRCOMP, the variation of the UVLO's preset thresholds  $V_{TH+}/V_{TH-}$  versus temperature is only 1.94 mV and 2.41 mV, respectively (Figs. 8b and 8c). As shown in Fig. 9, the critical temperature of the TSD is 89.6  $^{\circ}$ C and the temperature hysteresis window is  $\Delta T = 18$   $^{\circ}$ C, which is slightly different from the pre-set specification (20  $^{\circ}$ C). That is because the values of resistors  $R_{TS1}$ ,  $R_{TS2}$  and  $R_H$  (Fig. 5(b)) were selected based using a unit resistor of 78 k $\Omega$  to achieve a good layout for matching purposes. The TSD circuit maintains its targeted critical temperature trip point and temperature hysteresis window at different values of VDD, even that the supply voltage lower than  $V_{TH-}$  of the UVLO, thus ensuring the proper operation within the defined safe range of the VDD as defined by the UVLO ( $V_{DD} > 4.2$  V).

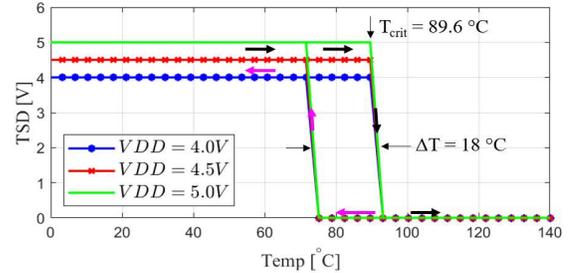


Fig. 9. TSD post-layout simulation results at different supply voltage.

Compared to the reported works in the literature [3,5-7], the accuracy of the proposed UVLO is around 2 mV for  $V_{TH+}$  and 2.5 mV for  $V_{TH-}$  that is much lower than the best work reported in [7] with 49 mV of variation. The current consumption of the UVLO is only 7.76  $\mu$ A as compared to the lowest reported work in [11] which consumes 12  $\mu$ A. The proposed TSD consumes 5.4  $\mu$ A with the area 0.0127 mm<sup>2</sup>, which is more compact than 0.078 mm<sup>2</sup> of the similar work reported in [8].

## V. CONCLUSIONS

This paper proposed a novel low- $I_Q$  bandgap comparator (BGRCOMP) with internal reference and its typical applications in designing UVLO and TSD circuits. By using the proposed low- $I_Q$  BGRCOMP, extra bandgap references inside UVLO and TSD circuits can be eliminated, thus, the static power consumption and silicon area can be significantly reduced. The post-layout simulation results show the best thermal drift of the UVLO compared to other works, with less than 3 mV for the UVLO, no change in the TSD trip points at different VDD, while it consumes less than 8  $\mu$ A of current for UVLO and 6  $\mu$ A for the TSD. The design areas are only 0.0083 mm<sup>2</sup> for UVLO and 0.0127 mm<sup>2</sup> for the TSD, smaller than that in other works with equivalent technologies.

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## REFERENCES

- [1] G. Rincon-Mora, "Analog IC Design with Low-Dropout Regulators (LDOs)", 2<sup>nd</sup> Edition, *McGraw-Hill Education*, 2014.
- [2] M. R. Hoque and S. S. Ang, "A CMOS under-voltage lockout circuit", in *Proc. World Congress on Engineering and Computer Science (WCECS)*, pp. 1-4, Oct. 2008.
- [3] K. Song, W. Oh, J. Choi, "A UVLO with Zero Static Power Consumption Power-on Reset Circuit in HVIC", in *Proc. Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, pp. 1085-1089, May 2017.
- [4] M. Cho et al., "Development of under-voltage lockout (UVLO) circuit configured Schmitt trigger", in *Proc. ISOC*, pp. 59–60, Nov. 2015.
- [5] Z. Yongrui and L. Xinquan: "Novel bandgap-based under-voltage-lockout methods with high reliability", *J. Semicond.*, vol. 34, no. 10, pp. 1-8, Oct. 2013.
- [6] W. Guo, S. Du, C. Bai, L. Lei, and Y. Zhu, "Design of a low temperature drift undervoltage lockout circuit-Used for GaN FET power driver IC", in *Proc. 15<sup>th</sup> SSL China: IFWS*, pp. 46-49, Oct. 2018.
- [7] H. Wu, M. Zhao, Z. Yang, S. Liu, and X. Wu, "Design of a Low Temperature Drift UVLO Circuit with Base Current Compensation", in *Proc. IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, pp. 1-3, Jun. 2019.
- [8] W. Ding, Y. Xu, R. Min, Z. Sun and Y.-L. Wu, "A Novel Thermal Protection Circuit Based on Bandgap Voltage Reference", in *Proc. 5<sup>th</sup> International Conference on Electronics, Communications and Networks (CECNet)*, pp. 43-50, Jun. 2016.
- [9] L. Q. Cartagena, S. E. Barbin, and W. J. Salcedo, "A New Sensor for Temperature Self-Protection of Integrated Circuits in CMOS Technology", in *Proc. IEEE MTT-S Latin America Microwave Conference (LAMC)*, pp. 1-4, Dec. 2018.
- [10] D. F. Lu and C. Hsia, "Over Temperature Protection Circuits for Integrated Power Converters", in *Proc. IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW)*, pp. 1-2, May 2018.
- [11] M. R. Hoque and S. S. Ang, "A CMOS under-voltage lockout circuit", in *Proc. World Congr. Eng. Comput. Sci. (WCECS)*, pp. 435-438, Oct. 2008.
- [12] G. C. M. Meijer, S. G. Wang, and F. Fruett, "Temperature Sensors and Voltage References Implemented in CMOS Technology", *IEEE Sens. J.*, vol. 1, no. 3, pp. 225-234, Oct. 2001.
- [13] K. A. A. Makinwa, "Smart temperature sensors in standard CMOS", *Procedia Eng.*, vol. 5, pp. 930-939, Sept. 2010.
- [14] D. M. Binkley, "Tradeoffs and optimization in Analog CMOS design", *John Wiley & Sons*, Aug. 2008.
- [15] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations", *IEEE J. Solid-State Circuits*, vol. 1, no. 3, pp. 224-231, Jun. 1977.
- [16] K. Isono, T. Hirose, K. Tsubaki, N. Kuroki and M. Numa, "A 18.9-nA standby current comparator with adaptive bias current generator", in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, pp. 237-240, Nov. 2011.
- [17] V. H. Nguyen, N. Ly, A. H. Alameh, Y. Blaquièrè, and G. Cowan: "A Versatile 200-V Capacitor-Coupled Level Shifter for Fully Floating Multi-MHz Gate Drivers", in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2021 (accepted).
- [18] N. Ly et al., "A High Voltage Multi-Purpose On-the-Fly Reconfigurable Half-Bridge Gate Driver for GaN HEMTs in 0.18- $\mu$ m HV SOI CMOS Technology", in *Proc. 18<sup>th</sup> IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, pp. 1-4, Aug. 2020.