

**Material Characterization of Self Assembled Copper-Silicide Nanostructures  
on Si(001), (110), and (111)**

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THESIS

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*To my wife and parents.*

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## LIST OF ABBREVIATIONS

BF	Bright Field
CMOS	Complementary Metal Oxide Semiconductor
DF	Dark Field
DOS	Density of States
DP	Diffraction Pattern
FIB	Focused Ion Beam
FFT	Fast Fourier Transform
FT	Fourier Transform
IPA	Isopropyl Alcohol
LDOS	Local Density of States
SEM	Scanning Electron Microscopy
STEM	Scanning Transmission Electron Microscopy
STM	Scanning Tunneling Microscopy
STS	Scanning Tunneling Spectroscopy
TEM	Transmission Electron Microscopy
XEDS	X-ray Energy Dispersive Spectroscopy
UHV	Ultrahigh Vacuum

## SUMMARY

The central aim of this thesis is to investigate the material and electrical properties of self assembled copper-silicide on silicon (001), (110), and (111) with electron beam evaporation in ultrahigh vacuum. In material characterization, copper-silicide phases and crystallographic direction were investigated. In electrical characterization, electrical resistivity, failure current density, current-voltage spectroscopy, and differential conductance spectroscopy were studied.

Metal silicide is a compound formed between a metal and silicon. It can possess a diverse range of properties, e.g. thermoelectric, semiconducting, optical, etc. Due to size effects, some of these properties are enhanced and may be of technological interest. For example, enhanced thermoelectric property in iron-silicide at nanoscale structures may be a potential replacement to current toxic and rare thermoelectric material like antimony and tellurium. Most investigations of metal silicides are usually centered on a few metals (e.g. iron, nickel, cobalt, titanium). However, copper is a common metal, non-toxic, and CMOS compatible. Yet, copper-silicide nanostructures are rarely studied. Most of the basic properties like material and electrical of copper-silicide are still from the thin film studies, which were conducted in the 1990s.

Copper silicide nanostructures are commonly fabricated by self assembly techniques because of the simplicity in the approach. The self assembly fabrication method used in this thesis was electron beam evaporation method, which has successfully fabricated self assembled silver nanowires on vicinal silicon before. Silver and silicon do not form a silicide and thus the silver nanostructures were monotectic. As such, the electron beam evaporation method may not be able to self assemble a silicide material like copper-silicide. Therefore, the first objective of this thesis was to demonstrate that the electron beam evaporation approach can fabricate self assembled copper-silicide nanostructures on silicon(001), (110), and (111).

## SUMMARY (continued)

The next objective was to study the material properties of the copper-silicide nanostructures. The foremost task was to determine the material composition of the nanostructures, since there are many copper-silicide phases. Using X-ray energy dispersive spectroscopy method, the nanostructures were found to possess a  $\text{Cu}_3\text{Si}$  phase. Since the self assembled nanostructures were single crystalline, the crystallographic orientation of the  $\text{Cu}_3\text{Si}$  was characterized with electron diffraction pattern. Although there are three different  $\text{Cu}_3\text{Si}$  polytypes, i.e.  $\eta$ ,  $\eta'$ , and  $\eta''$ , the former is the most fundamental and can be used for crystallography work. In this study, the growth directions of copper-silicide nanowires on silicon (001), (110), and (111) were either along the  $\eta\text{-Cu}_3\text{Si}[001]$  or  $\eta\text{-Cu}_3\text{Si}[100]$ .

The third objective of this thesis was to measure electrical resistivity, failure current density, and current-voltage spectroscopy of self assembled copper-silicide nanostructures. In the electrical resistivity work, one nanowire on silicon (111) and two nanowires on silicon (110) were measured with a four point probe. The resistivity ranged between  $30\text{-}50\mu\Omega\cdot\text{cm}$  and is consistent with other published works. However, there was no other published record on failure current density of copper-silicide nanowires. Here, the failure current density was plotted against different wire widths, and the bulk failure current density was estimated to be  $\sim 2 \times 10^7 \text{ A}\cdot\text{cm}^{-2}$ . The electrical characterizations above were conducted with a four or two point nanoprobe, which is limited to nanostructure with dimensions  $>100 \text{ nm}$ . Therefore, to study nanostructures  $<100 \text{ nm}$ , a scanning tunneling microscopy was used. The current-voltage spectroscopy from this study shows that the copper-silicide nanostructure with sub  $10 \text{ nm}$  heights behave as non-metallics, with more semi-metal or semiconducting behavior.

# 1. INTRODUCTION

## 1.1 Background and Motivations

A metal-silicide is a compound formed by alloying metal and silicon (Si) materials. It may possess several phases and its equilibrium phase depends on the stoichiometry and temperature of the mixture. Thin film metal-silicides have been intensively studied and characterized in the past. From thin film data, metal-silicides are generally metallic [1, 2] but other useful properties have also been discovered such as thermoelectric in  $\text{ReSi}_{1.75}$  [3, 4], photonic in  $\text{Mg}_2\text{Si}$  [5], semiconducting in  $\text{Ca}_3\text{Si}_4$  [6], and superconductivity in  $\text{LaSi}_2$  [7]. Metal silicides can be quite versatile with some exhibiting multiple properties. For examples,  $\text{FeSi}_2$  has both thermoelectric [8, 9] and photovoltaic [8, 10, 11] properties while  $\text{CrSi}_2$  has optical [12] and semiconducting [13] properties. These metal-silicides have a wide range of properties and have been proposed for use in diverse applications, e.g. thermoelectric and photovoltaic [14, 15]. Versatile properties are not the only advantage of metal silicides, they are also easy to fabricate. A simple metal deposition on Si with thermal annealing can transform them into a metal-silicide layer, see for example  $\text{FeSi}_2$  in Reference [16].

Progress in manufacturing technology allows metal silicides to be fabricated at the nanoscale regime. A nanostructure can be classified into 0-dimension (quantum dots), 1-dimension (nanowires) or 2-dimensions (atomically flat) structure. Many physical and chemical properties can be greatly enhanced when a structure is reduced to sufficiently small dimensions nanostructures. For example, Sun *et al.* in Reference[17] have predicted that Bi nanowires will have higher ZT (a figure of merit for thermoelectric) values than its bulk counterpart. The prediction is not limited to Bi only as similar size effect observations can also be seen in  $\text{CrSi}_2$  nanowires [18]. Another example is the transformation of metallic property in bulk  $\text{TiSi}_2$  to semiconducting property in nanostructure  $\text{TiSi}_2$  [19]. But a more intriguing observation is

that at the nanoscale level, metal silicides can exhibit new or novel properties that are not seen in bulk (thin film) structures. For instances, Seo *et al.* in Reference [20] reported unusual magnetic behavior seen in CoSi nanowires and novel semiconducting behavior in CrSi<sub>2</sub> nanowires was reported in Reference [21]. Therefore, studies of metal silicide nanostructures are important not only for research and development of nanoscale devices but also for discovery of new or novel properties. The latter is quite significant since new or novel property may offer a better (from performance and/or cost perspective) alternative to currently employed material. For example, enhanced ZT values of FeSi<sub>2</sub> nanostructures can potentially replace hazardous PbTe as a thermoelectric material. Although many metals will form metal silicides, to date, studies of metal silicide nanostructures are mostly focused on a few metals, e.g. nickel-silicide in Refs. [22-28], iron-silicide in Refs. [29-34], cobalt-silicide in Refs. [20, 28, 35-39], titanium-silicide in Refs. [40-44], and tantalum-silicide in Refs. [45-47]. The aforementioned metals are all CMOS compatible [48], which may explain the reason for their interest and intensive studies. However, there are other metals such as Cu, which is deemed more common than the abovementioned metals. Cu is widely available, CMOS compatible and has a low electrical resistivity ( $\sim 1.54 \mu\Omega\cdot\text{cm}$  [49]). As such, Cu is currently used as a material in IC interconnects [50, 51]. Therefore, Cu may be of research interest since Cu diffuses easily into Si and also forms copper-silicide (Cu-Si) [52]. Historically, a damascene technique was introduced to prevent the diffusion and Cu-Si formation of Cu interconnects in Si [53-55]. Nevertheless, the constituents of Cu-Si, i.e. Cu and Si, are non-toxic and therefore use of Cu-Si will be in compliance with the environmental protection agency (EPA) green movement [56-58]. Use of copper-silicide (Cu-Si) nanostructures is compatible with the current CMOS facility and complies with EPA goals and therefore has limited manufacturing implementation obstacles.

Cu-Si is generally an ohmic material with electrical resistivity ranging between 20-60  $\mu\Omega\cdot\text{cm}$  for thin films [59] and nanowires [60]. However, recent studies on Cu-Si nanostructures have revealed



existence of other properties and uses as well. Yuan *et al.* in Reference [61] reported that Cu-Si nanostructures also possessed novel optical properties. Wen *et al.* in Reference [62] shown that Cu-Si nanostructures can be used as a catalyst to fabricate Si nanowires. Si nanowires are versatile component of nanotechnology, which can be used for photovoltaics [63, 64], thermoelectrics [65], biosensors [66], chemical sensors [67], and anode materials for Li-Ion batteries [68]. Most of these aforementioned characteristics are dependent on a more fundamental property of the Cu-Si nanostructures, which is the crystallography. Since the growth of Si nanowires on Cu-Si nanostructures is heteroepitaxial [62], the crystallographic orientation of the self assembled Cu-Si nanostructures will depend on the Si surface periodicities. The ability to control the crystallographic orientation of a nanostructure is important because it will then allow us to engineer or design the characteristics of the nanostructure. Therefore, understanding the crystallographic orientation of self assembled Cu-Si nanostructures on different Si surface periodicities is an important aspect of materials characterization and will be a focus of this thesis work.

Crystallography of Cu-Si nanostructures on Si were investigated by Zhang *et al.* in Reference [69], where they proposed a chemical vapor deposition (CVD) method to self assemble Cu-Si nanostructures on Si(001), Si(110), and Si(111) using Au nanoparticles as a catalyst. The growth method produces planar (or horizontal) nanowires on a Si(110) substrate, whereas triangle and square nanoislands will form on Si(111) and Si(001), respectively. A variation of the CVD method without Au catalyst was proposed by Li *et al.* in Reference [70]. The authors deposited Cu or CuO vapor on a SiO<sub>2</sub>/Si(001) substrate to fabricate self assembled Cu-Si planar nanowires. An advantage of the last approach is that the Cu-Si nanostructures can transform into different shapes (nanoscale triangle, square, and wire structures) by controlling its annealing temperature. However, the annealing time given in the paper had a wide margin, i.e. 0.5 – 5 hours. Both of the aforementioned methods fabricate Cu-Si nanostructures atop Si and

employ foreign elements, i.e. Au and O, in their fabrication processes. Au is not CMOS compatible and thus it cannot be adopted in CMOS facility. O may also react with the metal silicide nanowire [71-73]. As a result, the nanostructure composition, phase, and growth mechanics may be altered and may no longer represent the ideal self-assembled Cu-Si nanostructure on Si. As this work is focused on the fundamental properties of nanoscale Cu-Si nanostructure, a research objective was to study the basic properties of ideal Cu-Si nanostructures, i.e. Cu-Si single crystalline nanostructures without the presence of foreign elements. Thus, the self-assembly of Cu-Si nanostructure with e-beam evaporation in an ultrahigh vacuum environment was chosen as the fabrication method and will be discussed in detail in Chapter 2.

## 1.2 Goal and Objectives

The goal of this thesis is to study the fundamental properties of self assembled Cu-Si nanostructures on Si fabricated by e-beam evaporation method in UHV. The e-beam approach was pioneered by Roos *et al.* in Reference [74] and Stalhmecke in Reference [75] to self assemble Ag nanowires on vicinal Si(001). The method employs evaporated Ag particles to deposit onto a heated ( $\sim 600$  °C) Si substrate in UHV. After a period of time, e.g. 30 minutes, Ag nanostructures will form on the Si surface. Therefore the fabricated Ag nanostructures are monotectic [76] and grew atop the Si via step bunching method [74]. While the fabrication and growth mechanics of self assembled Ag nanowires on vicinal Si(001) were studied, there was no published record on the growth mechanics and experimental work of self assembled Cu-Si nanostructures on Si. Hence, we are uncertain if the e-beam evaporation method in UHV would result in self assembled Cu-Si nanostructures on Si(001), Si(110), and Si(111). Therefore the first objective of this thesis is to demonstrate that self assembled Cu-Si nanostructures can be fabricated atop Si(001), Si(110), and Si(111), which will be discussed in Chapter 2.

The second objective was to study the material properties of the Cu-Si nanostructures and this will be discussed in detail in Chapter 3. Since the self assembly process selected to fabricate Cu-Si had not been used by other researchers, the material composition needed to be studied in order to verify the Cu-Si phase of the fabricated nanostructures. It was expected, based on Cu-Si phase diagram [77], that the Cu-Si nanostructures phase would be  $\text{Cu}_3\text{Si}$ , and experimental studies were used to corroborate the prediction. The material composition of the nanostructures was characterized with X-ray energy dispersive spectroscopy (XEDS) in a transmission electron microscope (TEM). The  $\text{Cu}_3\text{Si}$  crystalline in the self assembled Cu-Si nanostructures was also predicted to be influenced by the surface periodicities of the Si substrate, i.e. heteropitaxy. Therefore, the crystallographic orientation of Cu-Si nanostructures on Si(001), Si(110), and Si(111) was also studied with electron diffraction pattern (DP) in a TEM.

In the third objective of this thesis, the electrical properties of Cu-Si nanostructures were investigated and will be discussed in Chapter 4. Prior studies on  $\text{Cu}_3\text{Si}$  have revealed that the thin film electrical resistivity is  $\sim 30 - 60 \mu\Omega\cdot\text{cm}$  [59, 78] while nanowire electrical resistivity is  $\sim 21 \mu\Omega\cdot\text{cm}$  [60]. For the latter, the authors attributed their lower resistivity to single crystalline material, which has reduced electron scattering. Nevertheless, the Cu-Si nanowires in Reference [60] were free standing and grew along the  $\langle 001 \rangle$   $\eta$ -  $\text{Cu}_3\text{Si}$  direction. However, we expect that the Cu-Si nanowires that self assemble on Si(001), Si(110), Si(111) to have different crystallographic orientation and, thus, may possess a different electrical resistivity [79]. To the best of our knowledge, there are no published reports on failure current density of a single crystalline Cu-Si nanowire. Therefore, the failure current density of Cu-Si nanowires was also investigated because it is of technological interest [80]. For electrical resistivity, *in situ* four point probe method was used to preserve the pristine nature of the nanowire and directly measure the electrical resistance of the Cu-Si nanostructures. In electrical current stressing experiments, an electrical current was injected into Cu-Si nanostructures via a two point probe method. The above method employs

nanoprobes to physically contact the Cu-Si nanostructures, which is usually limited to probe nanostructures of dimensions  $> 100$  nm. Therefore, to electrical characterize sub 100 nm Cu-Si nanostructures, a scanning tunneling microscopy (STM) for electrical resistivity characterization (via density of states data).

During the investigation for the second objective, the Cu-Si nanostructures on Si were discovered to react rapidly with the ambient oxygen. One of the interesting result of the oxidation was the anisotropic etching effects on the Si(001) underneath the Cu-Si nanostructures, which formed a v-channel along the Si{111}. Although oxidation of thin film Cu-Si has been studied by several researchers [73, 78], the anisotropic etching effect on Si(001) due to nanoscale structure has not been reported before. Therefore, the chemical composition of this oxidization process could be different those reported in the aforementioned references. Furthermore, the nanoscale Cu-Si etching on Si was entirely solution free and therefore there may a potential interest to utilize this method in nanofabrication technology. Thus, the oxidation of Cu-Si nanostructures on Si was material characterized with XEDS and high resolution TEM (HRTEM), which is discussed in Chapter 5.

Another interesting discovery was made during investigating the third objective. It appeared that e-beam evaporation of Cu onto Si(110) changes the Si surface significantly. The resultant Cu deposition would reconstruct the clean Si surface into a long range order  $2.3 \times 2.3$  superstructure. Si surface reconstruction due to metal were studied in the past, e.g. see for example due to Ni [81-83], due to Ag [84], and due to Cu [85]. However, none of the reported surface reconstruction matches the observation in this experimental work. Therefore, Chapter 6 will discuss the experimental work and results that produced a different surface reconstruction of Si(110) due to Cu deposition. Finally, Chapter 7 will include a discussion of conclusions and future work.

## **2. FABRICATION OF SELF ASSEMBLED CU-SI NANOSTRUCTURES**

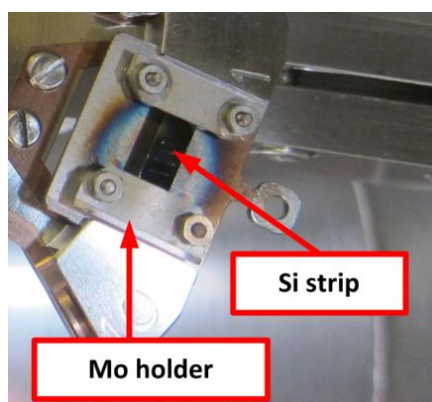
### **2.1 Introduction**

As stated in previously, prior research on self assembly of nanostructures with e-beam evaporation in UHV had focused on Ag nanostructures on vicinal Si(001), see for example Reference. [74, 75, 86]. The fabricated Ag nanostructures on Si are monotectic, which is consistent with non soluble Ag-Si phase [76]. As such, Ag does not form a metal silicide nor diffuses into Si. Therefore, the Ag adatoms can remain mobile on the Si surface. The Ag adatoms tend to nucleate and step bunch along vicinal Si steps that may lead to self assembly of nanostructures [74]. The first objective of this thesis research was thus to test the hypothesis that self assembly of nanostructures with e-beam evaporation in UHV is possible, even for metals that are soluble and form silicides. Due to limited research on Cu nanostructures on Si, which readily forms Cu-Si and diffuses easily into Si [87], it is expected that the growth mechanics for Cu-Si nanostructures on Si will be different from that of self assembled Ag nanostructures on vicinal Si(001). Hence, this chapter investigates the self assembly of Cu-Si nanostructures by e-beam evaporation on different crystallographic Si substrates, namely Si(001), Si(110) and Si(111).

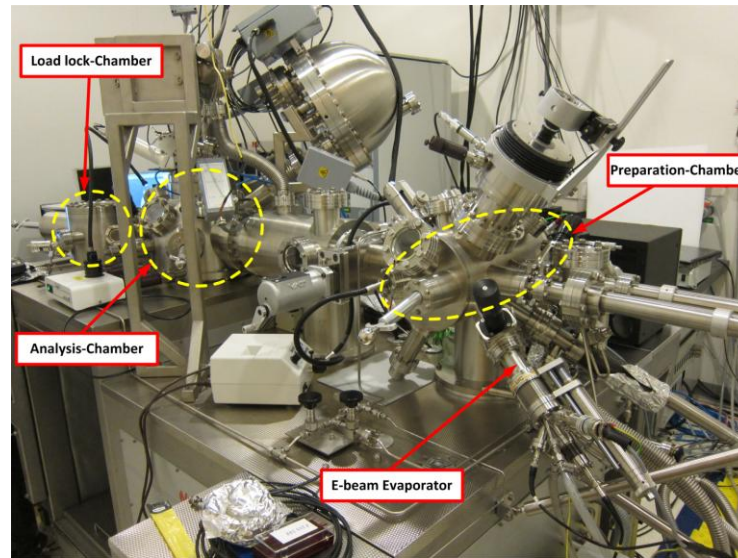
### **2.2 Fabrication Procedures**

Fabrication of self assembled Cu-Si nanostructures were performed on three different crystallographic orientation Si wafers, i.e. Si(001), Si(110), or Si(111), with 1-10  $\Omega\cdot\text{cm}$  resistivity. Prior to Cu deposition, Si wafers were cut into strips of  $\sim 10\text{ mm} \times 3\text{ mm} \times 0.5\text{ mm}$ . Each Si strip was cleaned with organic solvents, an acetone rinse followed isopropyl alcohol (IPA) before mounting into a Molybdenum holder (see Figure 1). The holder with a mounted Si strip was inserted into a load lock to transfer into a UHV chamber inside the Omicron Nanotechnology system (see Figure 2). The Omicron

system is located at the Center for Nanoscale Materials (CNM) in Argonne National Laboratory (ANL), IL and is comprised of two main ultrahigh vacuum (UHV) chambers; one is dedicated for fabrication (or preparation) while the other is for chemical analysis. Hence, the former is known as a preparation-chamber and the latter is known as an analysis-chamber. In the preparation-chamber, the Si strip was degassed at 600°C for at least 12 hours to remove unwanted hydrocarbons from the surface. A flash-heat treatment at 1200°C for 30 seconds was then performed five times to remove the native oxide on the surface.



**Figure 1:** A picture of a Mo holder to mount Si strip.



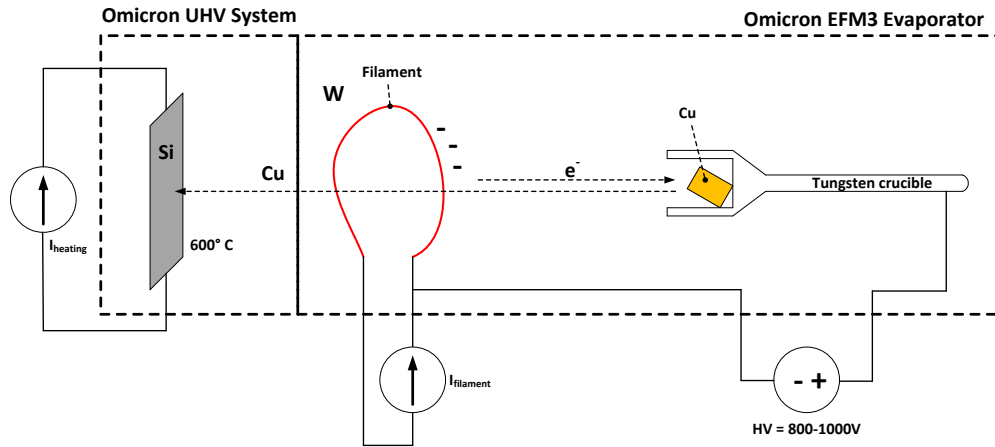
**Figure 2:** An overview picture of the Omicron Nanotechnology System in the CNM at ANL. The system consists of two UHV chambers, i.e. (1) a preparation-chamber for fabrication of self assembled Cu-Si nanowires and (2) an analysis-chamber for SEM characterization.

After degassing and flash-heating, Cu pellets of 99.999% purity from Kurt J. Lesker Co. were evaporated using a 2  $\mu\text{m}$  flux current with an e-beam evaporator for about 30 minutes. Figure 3 shows a simple construction of the evaporator used, i.e Omicron model EFM3. There are two power supplies to control the evaporation process that are labeled as HV and  $I_{\text{filament}}$ . A tungsten (W) filament is heated by the electrical current ( $I_{\text{filament}}$ ) to generate free electrons. The potential difference between the heated filament and the W crucible accelerates the free electrons to the Cu pellet inside the W crucible. Continuous bombardment of electrons on the Cu pellets will generate heat until the Cu evaporates. The evaporated Cu will travel (without scattering) to the Si sample, which is electrically heated at 600°C. The

electrical current to heat the Si is controlled by the  $I_{\text{heating}}$  power supply. In this thesis, the following parameters are typical used for e-beam evaporation of Cu on Si with an approximate 1-2 nm average surface coverage of Cu-Si nanostructures (both nanowires and nanoislands): HV=800-1000V,  $I_{\text{filament}} = 2\text{A}$ ,  $I_{\text{emission}} = 17\text{-}20\mu\text{A}$ , UHV pressure  $< 10^{-9}\text{mbar}$ .

It should be noted that the Cu flux cannot be calibrated with the HV or  $I_{\text{filament}}$  power supplies. As such, Cu flux is not a good quantitative measure of the fabrication results. Instead, an average surface coverage of the nanostructures is used, which is approximated by (average height of nanostructures) $\times$ (area coverage of nanostructures)  $\div$  (total area). The average height is obtained from TEM micrographs whereas the area coverage is computed from SEM data. The analysis-chamber has a scanning electron microscope (SEM) for inspecting and analyzing the fabricated nanowires.



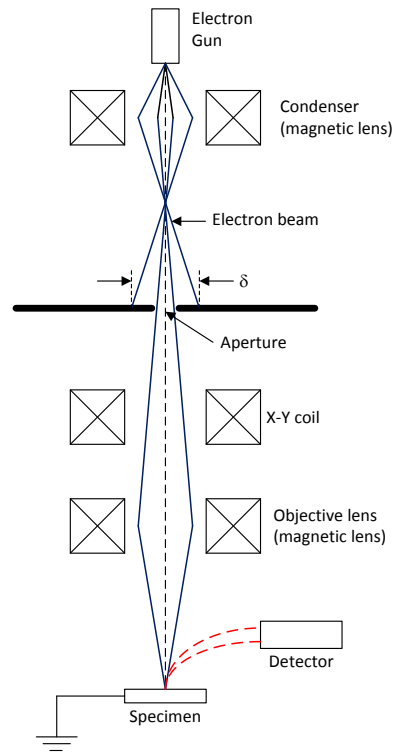


**Figure 3:** A simplified schematic of an electron beam evaporation process. The Omicron EFM3 evaporator and the Omicron UHV system are connected and are at UHV. The evaporator is comprised of a filament and crucible. Cu pellets in the crucible are evaporated by an e-beam from the heated filament. The e-beam is controlled by two external power supplies,  $I_{\text{filament}}$  and HV. The evaporated Cu will deposit onto a heated Si sample, which is controlled by an external power supply,  $I_{\text{heating}}$ .

### 2.3 In Situ Scanning Electron Microscopy Imaging

*In situ* scanning electron microscopy (SEM) imaging was performed to verify the results of e-beam evaporation of Cu onto Si. The SEM is a part of the Omicron system shown in Figure 2. Since the SEM is connected to the same UHV as the e-beam evaporator, the Si sample was never removed from the Omicron system. Hence, the SEM imaging was *in situ*. A typical SEM is an imaging instrument to view specimens with dimensions in the micrometer or nanometer range [88]. A simplified schematic of an SEM is shown in Figure 4, which is comprised of an electron gun, a condenser, an aperture, an X-Y coil,

an objective lens, and a detector [88]. The purpose of the electron gun is to emit an electron beam and control the electron beam voltage. The beam width,  $\delta$ , at the aperture is controlled by the condenser, which in turn controls the beam current on the specimen. After passing through the aperture, the electron beam is deflected by the X-Y coil to move the beam laterally in the x-y directions on the sample. The focal point of the beam is adjusted by an objective lens. The detector in a SEM senses electrons from back scattering and secondary scattering effects, which are later (either or both scatterings) processed into SEM images in a computer. The quality of the image depends on the electron beam's voltage and current. Higher voltage and current will result in higher quality but will damage the sample [89]. Also, the SEM specimen must be grounded to avoid Coulomb charging that will distort the SEM image [90]. However, insulating materials, e.g. an oxide layer, are difficult to ground and thus will inevitably result in distorted SEM images.



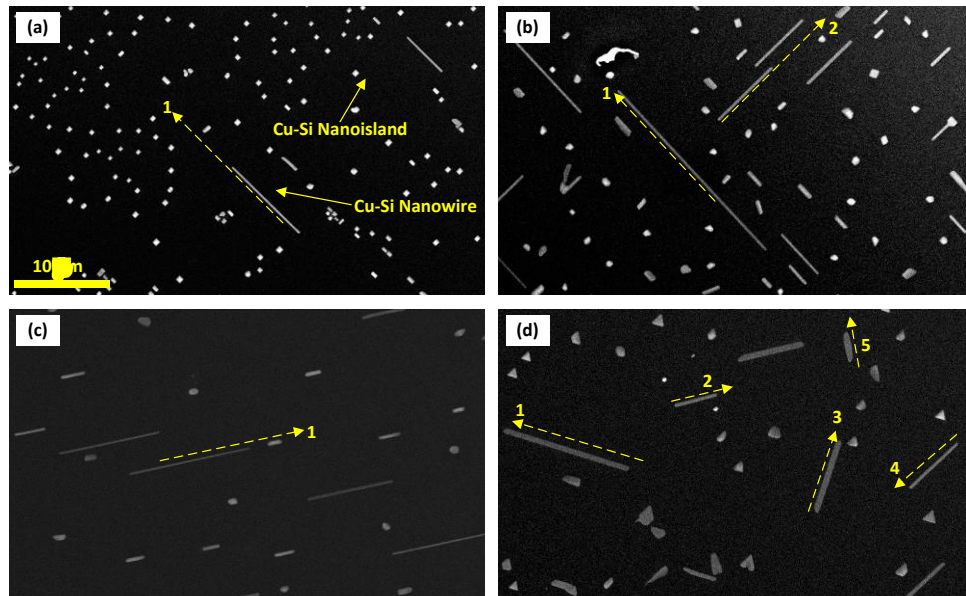
**Figure 4:** A simplified schematic of a scanning electron microscope (SEM). Electrons are emitted from the electron gun. The electrons are treated as an electron beam (blue lines) that is controlled by a condenser, an X-Y coil, and an objective lens. Interaction between the electron beam and specimen will result in electron back scattering and secondary scattering (red dashed lines), which are sensed and amplified by the detector.

## 2.4 Results and Discussion

Figures 5(a)-(d) show *in situ* SEM micrographs of e-beam evaporation of Cu onto a  $4^\circ$  miscut vicinal Si(001), a flat ( $<1^\circ$  miscut) Si(001), a flat ( $<1^\circ$  miscut) Si(110), and a flat ( $<1^\circ$  miscut) Si(111), respectively. The physical dimension of these nanostructures differs greatly. For nanowires, their diameter ranges from 50 nm to several hundreds of nm. Smaller diameters  $< 50$  nm are possible but would be difficult to observe with a SEM and as will be discussed in Chapter 4, where the results of nanostructures with sub10 nm dimensions observed with STM are presented. The length of these nanowires ranges from few microns to few hundreds of microns, depending on the Si substrates. The Cu-Si nanoislands can have various shapes as well. Square and rectangular nanoislands were more common on Si(001) samples. Cu-Si nanoislands on a Si(110) tend to elongate along the same direction as the nanowires. Triangle nanoislands were common on a Si(111) but other undefined (random) shapes were observed as well. From the micrographs, the physical traits of the Cu-Si nanowires and nanoislands appear to depend on the type of Si substrate, i.e. (001), (110), and (111). However such observations will need to be corroborated in future studies.

A main difference between the growth results on the four substrates is the direction of the Cu-Si nanowires, as indicated by the yellow dashed arrows in the figures. The numeric label in the figures shows the number of directions found on the micrograph. On a vicinal Si(001), the Cu-Si nanowires grew in one direction whereas on a flat Si(001), the nanowires grew in two perpendicular directions. Self assembled Cu-Si nanowires grew only in one direction on a Si(110) sample. Cu-Si nanowires grew along five directions on a Si(111). However, a Si(111) surface has a six fold symmetry, i.e. three directions along  $\{110\}$  and another three directions along  $\{112\}$ . Therefore, the sample size in Figure 5(d) may not be large enough to capture all six directions. The growth directions of Cu-Si nanowires on Si(001),

Si(110), and Si(111) will be further analyzed in the material characterization and discussion found in Chapter 3.



**Figure 5:** Typical results of Cu deposition on (a) a 4° miscut vicinal Si(001), (b) flat (<1° miscut) Si(001), (c) Si(110), and (d) Si(111). Self assembled Cu-Si nanowires and nanoislands can be seen on all cases. Numeric label besides a dashed arrow gives a count of the growth nanowire direction found on the sample with (a) one direction, (b) two perpendicular directions, (c) one direction, and (d) five directions.

## 2.5 Summary

Self assembled Cu-Si nanostructures were successfully fabricated on Si(001), Si(110), and Si(111) using e-beam evaporation method in UHV. On each Si substrate, the Cu-Si nanostructures grew differently. In particular, the Cu-Si nanowires grew in different directions. We can assume that such results were due to the surface properties of Si substrates. To verify this assumption, a high resolution analysis on cross section Cu-Si nanostructures will be needed, which will be discussed in Chapter 3. However, the growth mechanics of the self assembled Cu-Si nanostructures were not studied. Therefore a future work will be needed to explore the growth mechanics.

### **3. MATERIAL CHARACTERIZATION OF THE STRUCTURE AND COMPOSITION OF SELF ASSEMBLED CU-SI NANOSTRUCTURES**

#### **3.1 Introduction**

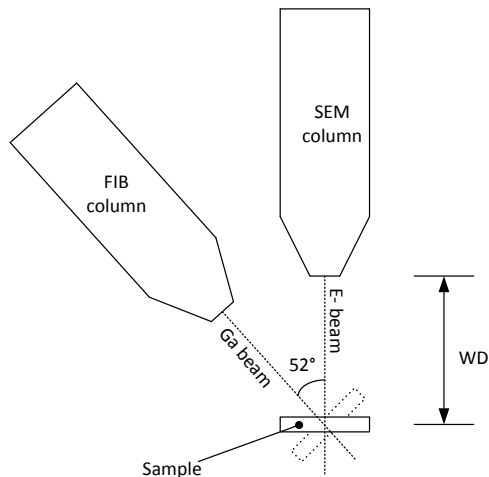
The second objective of this thesis was to study the material composition (phases) and crystallographic directions of the self assembled Cu-Si nanostructures. Since the self assembly of Cu nanostructures with e-beam evaporation was a new approach, fundamental information on the composition and atomic structure was unknown. Thus, the research aim was to characterize these aforementioned material properties for self assembled Cu-Si nanostructures on Si(001), Si(110), and Si(111) in order to study substrate effects. During the e-beam evaporation, the amount of Cu precipitated is very small as compared to the amount of Si. Therefore, based on the Cu-Si phase diagram and annealing temperature of 600°C, the expected first equilibrium phase from the deposition is Cu<sub>3</sub>Si [77]. In this chapter, XEDS was used to measure the composition of self assembled nanowires on Si. Since the nanowires were self assembled, we can expect that they will be single crystalline as observed for the Ag self assembled nanostructures. Electron diffraction pattern (DP) was employed to characterize the crystallographic orientation of the Cu-Si nanostructures. Both XEDS and electron DP are a part of the transmission electron microscope (TEM), which operates by transmitting electron through an ultrathin sample. As such, ultrathin TEM specimens of the Cu-Si nanostructures were prepared with focused ion beam (FIB) cutting.

## **3.2 Experimental Procedures**

### **3.2.1 Focused Ion Beam Prepared TEM Specimen**

The focused ion beam (FIB) in this thesis is a dual FIB/SEM beam FEI Nova 600 NanoLab model, which is located at the CNM, ANL, IL. The FIB system employs a gallium (Ga) ion beam [91]. Since the Ga beam is a stream of charged particles, the basic operation of FIB is very similar to that of a SEM. Because Ga is a heavy element, a Ga beam can easily remove atoms from a solid material upon contact. Therefore, imaging with FIB is quite damaging to the sample. Instead, FIB is designed for ion milling and cutting of samples for nanofabrication. In this thesis, a FEI Nova 600 was used and is schematically illustrated in Figure 6. The Nova system has two beam columns that are separated by an angle of  $52^\circ$ . The point where the two beams coincide is called the eucentric height, which is measured from the specimen surface to the SEM cone tip. The work-distance (WD) adjusts the specimen height and is set at the eucentric height so that the specimen can be switched between the SEM and FIB by rotating the sample  $52^\circ$ .





**Figure 6:** A schematic illustration of a dual beam FIB/SEM system with two ion columns separated by a  $52^\circ$ . The work distance, WD, is adjusted along the SEM column direction only. The substrate (sample) can be rotated to be perpendicular to the Ga beam.

The FIB also has a gas injection system (GIS) that delivers organometallic platinum (Pt) gas for platinum deposition on the sample. Reaction between the gas and any ion beam (electron or Ga) will decompose the gas and condense Pt onto the surface [92]. This enable fabrication of Pt interconnects or Pt films. The latter serves as a protective layer from ion beam damages.

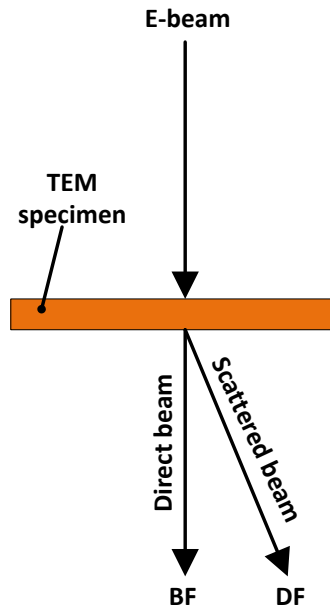
The procedure to prepare a TEM specimen with a FIB is briefly outlined here. First, a substrate (where the nanostructures self assembled) is set at WD = eucentric height. Then, a Pt layer  $>0.5 \mu\text{m}$  is deposited on the nanostructure. Afterwards, the substrate is rotated  $52^\circ$  to be perpendicular to the FIB. Then, an additional layer of  $>1 \mu\text{m}$  Pt layer is deposited with the Ga ion beam atop the existing Pt layer (from the previous e-beam deposition). This ion beam deposition is to increase the thickness of the Pt

layer to protect the specimen before cutting. It may be noted that Pt deposition with a Ga beam is much faster than the e-beam. Finally, the Ga beam cutting is performed. A cross section of the Pt protected nanowire is cut and transferred to a Mo TEM grid. It may be noted that due to the delicate process of Ga beam cutting, only larger nanostructures, e.g. nanowires, were selected for material characterizations in this chapter. After transferring the TEM specimen on the Mo grid, more milling was performed to further reduce the specimen thickness to an ultrathin layer of  $< 100$  nm. After that, the specimen is ready for TEM.

### **3.2.2 Transmission Electron Microscopy**

The basic operation of a transmission electron microscope (TEM) is also very similar to that of an SEM. However, instead of detecting electrons from back scattering and secondary scattering, a TEM detects transmitted electrons that have passed through the specimen (see Figure 7) [88]. Since the electron beam can leave the specimen via a direct or scattered electron beam, a TEM has two dedicated detectors for these two different beams [93]. Direct beam detection will show bright field (BF) images while scattered beam detection will show dark field (DF) images. Assuming a uniform thickness of a specimen, BF images will show darker area in region with heavier elements or higher density of atoms and vice versa for DF images. In this thesis, BF images are more frequently employed. Unless otherwise specified, all TEM micrographs presented in this thesis are BF.

TEM experiments conducted in thesis were performed with a JEOL JEM 3010 located at the University of Illinois at Chicago and a Tecnai F20ST AEM located at the Electron Microscopy Center (EMC), ANL. Both of these TEMs were used for XEDS and electron DP.

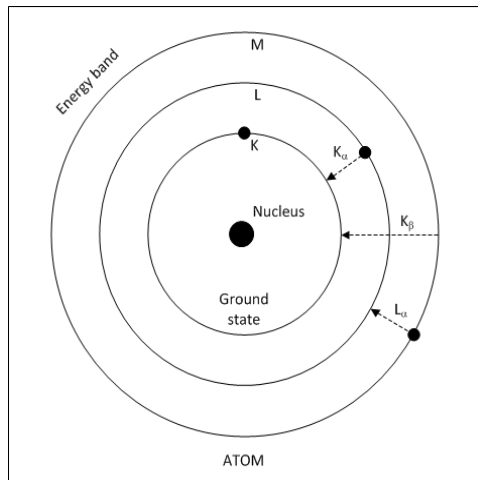


**Figure 7:** An illustration of a transmission electron microscope operation in bright field (BF) or dark field (DF) mode.

### 3.2.3 Material Composition with XEDS

X-ray emission resulting from an inelastic scattering of electrons with an atom(s) can provide an energy signature of the atom [93]. This technique is known as X-ray energy dispersive spectroscopy. X-ray spectroscopy has various acronyms, e.g. EDAX, EDX, EDS, or XEDS. This thesis adopts the latter acronym. During an inelastic scattering, an electron(s) in an atom will be excited to different energy bands, i.e. K, L, and M (with K being the innermost shell while M being the outermost shell) [94] as shown in Figure 8. When the excited electron(s) return to its K shell, it will emit X-ray energy. Since each atom has its own distinctive energy emission, identification of an unknown material is possible. This

identification is usually performed with software (this thesis uses ES vision 4.0 from Emispec System Inc.).



**Figure 8:** A simplified view of electron orbital energy levels with K, L, and M bands around an atomic nucleus.

#### **3.2.4 Crystallography with Electron Diffraction Pattern**

Electron diffraction pattern (DP) was employed to characterize the crystallographic orientation of the Cu-Si nanowires on Si(001), Si(110), and Si(111). A single crystalline material consists of atoms arranged in a periodic manner. When an electron beam passes through the periodic structure, the beam will be diffracted [95]. The diffraction can be analyzed with the Fourier method, which converts the real

lattice into the reciprocal lattice or  $\vec{k}$  space. If  $\vec{a}_n$  is a primitive vector in real space, where  $n = 1, 2$ , and  $3$ , then the reciprocal lattice is given as follows [96].

$$\vec{b}_1 = 2\pi \frac{\vec{a}_2 \times \vec{a}_3}{\vec{a}_1 \cdot (\vec{a}_2 \times \vec{a}_3)}, \vec{b}_2 = 2\pi \frac{\vec{a}_3 \times \vec{a}_1}{\vec{a}_2 \cdot (\vec{a}_3 \times \vec{a}_1)}, \vec{b}_3 = 2\pi \frac{\vec{a}_1 \times \vec{a}_2}{\vec{a}_3 \cdot (\vec{a}_1 \times \vec{a}_2)} \quad (1)$$

where ' $\times$ ' is a cross product and ' $\cdot$ ' is a dot product. It may be noted that the ' $hkl$ ' refers to atomic planes in Miller indices, which are defined as  $h\vec{a}_1 + k\vec{a}_2 + l\vec{a}_3$ . The  $\vec{k}$  space equivalence of these atomic planes are  $u\vec{b}_1 + v\vec{b}_2 + w\vec{b}_3$ .

A diffracted beam obeys Bragg's Law (or the Von Laue Formulation), which is given by the following formula [96].

$$n\lambda = 2d \sin \theta_B \quad (2)$$

$\theta_B$  is the Bragg angle,  $n = 1, 2, 3, \dots$ ,  $\lambda$  is the incident plane's wavelength, and  $d$  is the spacing of atomic planes. If Equation 2 is written in a 3-dimensional vector form, a crystal structure can be derived from the 3-D diffraction patterns. However, the pattern does not reveal the atomic elements. Therefore, another formula is used for this identification purpose and it is called the structure factor,  $F(\theta)$ , which is given as [93, 96],

$$F(\theta) = \sum_i f_i \exp[2\pi j(hx_i + ky_i + lz_i)] \quad (3)$$

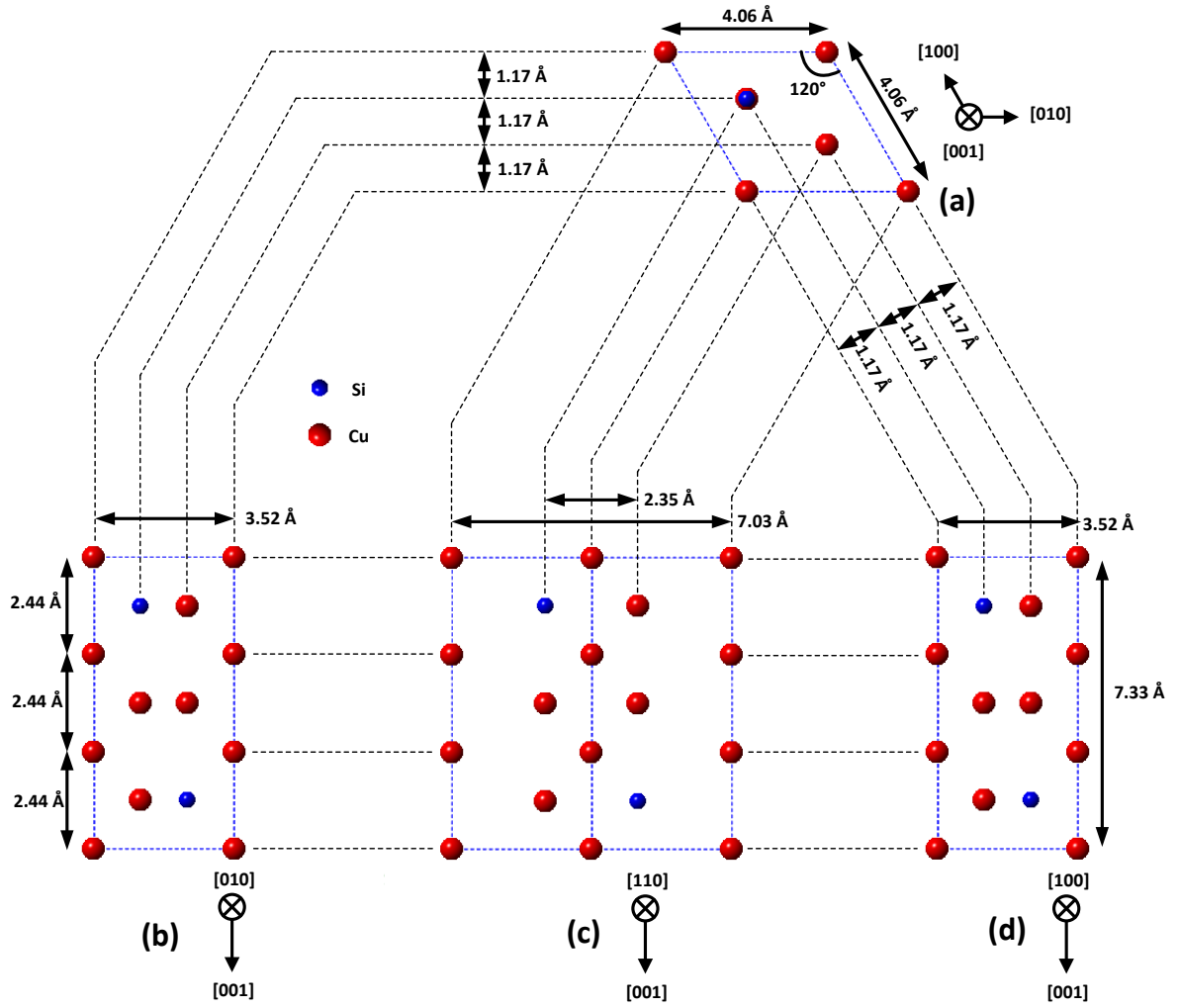
where,  $f_i$  = atomic form factor, which depends on the internal structure of the ion.  $F(\theta)$  in Equation 3 is a diffraction intensity that can reveal the atomic identity of a diffracted crystal.

However, there are three polytypes of  $\text{Cu}_3\text{Si}$ , i.e.  $\eta$ ,  $\eta'$  and  $\eta''$ - $\text{Cu}_3\text{Si}$ , each stable for certain temperature ranges [77]. Since the fabrication process involves annealing Si at  $600^\circ\text{C}$  during the Cu

deposition, the  $\eta$ -Cu<sub>3</sub>Si phase is predicted [77]. However, when the substrate is cooled, the Cu<sub>3</sub>Si phase may undergo phase transformation to  $\eta'$  or  $\eta''$  phases, whereby the latter exists at room temperature (RT) [97]. Since the  $\eta$ -Cu<sub>3</sub>Si is the fundamental structure for the  $\eta'$  and  $\eta''$  phases, we can use the  $\eta$  phase as a basis to analyze the crystallographic orientation of the self assembled Cu-Si nanowires [97, 98].

### 3.3 Structure of $\eta$ -Cu<sub>3</sub>Si

The  $\eta$ -Cu<sub>3</sub>Si data was imported from the Inorganic Crystal Structure Database (ICSD) [99] in the form of crystallographic information framework (CIF), which can be simulated with CrystalMaker® and SingleCrystal 2® [100]. Figures 9(a)-(d) show the  $\eta$ -Cu<sub>3</sub>Si crystal structure from CrystalMaker® using a  $hkl$  coordinate and are projected along  $[001]_{\text{Cu-Si}}$ ,  $[010]_{\text{Cu-Si}}$ ,  $[110]_{\text{Cu-Si}}$  and  $[100]_{\text{Cu-Si}}$  directions, respectively. The symmetry of the crystal structure belongs to  $P\bar{3}m1$ , which has a trigonal basis. When a  $hkl$  coordinate is used on a trigonal structure, not all the fundamental axes will be orthogonal, i.e.  $[100]_{\text{Cu-Si}} \perp [001]_{\text{Cu-Si}}$ ,  $[001]_{\text{Cu-Si}} \perp [010]_{\text{Cu-Si}}$  and  $[100]_{\text{Cu-Si}} \angle [010]_{\text{Cu-Si}}$  is  $120^\circ$ . The lattice constants of  $\eta$ -Cu<sub>3</sub>Si are 4.06 Å, 4.06 Å, and 7.33 Å along  $[100]_{\text{Cu-Si}}$ ,  $[010]_{\text{Cu-Si}}$ , and  $[001]_{\text{Cu-Si}}$ , respectively. The  $\eta$ -Cu<sub>3</sub>Si crystal structure simulated with CrystalMaker® can also be exported to SingleCrystal® to simulate electron DP for that particular orientation. Therefore, the simulation results were used for verifying the experimental TEM DP and to understand the crystallographic orientation of the nanostructures.



**Figure 9:** Atomic structure of the  $\eta$ -Cu<sub>3</sub>Si viewed along the following directions; (a) [001]<sub>Cu-Si</sub>, (b) [010]<sub>Cu-Si</sub>, (c) [110]<sub>Cu-Si</sub> and (d) [100]<sub>Cu-Si</sub> directions. The red atoms are Cu while the blue atoms are Si.

### 3.4 TEM Results and Discussion

#### 3.4.1 Self Assembled Cu-Si Nanowires on Si(001)

Two TEM specimens of self assembled Cu-Si nanowires on Si(001) fabricated under the same conditions (see Section 2.2.3) are analyzed in this section. Figure 10a is a TEM cross section view of a self assembled Cu-Si nanowire (first specimen) on a vicinal Si(001). The specimen was obtained from a nanowire indicated by a black line as shown in the inset of Figure 10a. Referring to the TEM micrograph, on the right hand side of the nanowire, the bright contrast region was amorphous suggesting the presence of oxygen. This was confirmed by XEDS data that showed an atomic ratio of O:Si:Cu = 44:33:24. The origin of the amorphous layer is not certain as it could be a result of exposure to oxygen during sample preparation and handling. As a comparison, XEDS measurements within the crystalline region shows an atomic ratio of O:Si:Cu = 9:24:67. In this case, the presence of low amount of oxygen is not uncommon due to native oxide found on the Si surface. If so, the oxygen reading within the crystalline region could be ignored. As such, the Cu:Si ratio becomes approximately 3:1, which suggests a Cu<sub>3</sub>Si phase. However, XEDS on other Cu-Si nanowires have revealed two unstable CuSi and Cu<sub>3</sub>Si<sub>7</sub> phases coexisting with Cu<sub>3</sub>Si phase as well [101]. The unstable phases may be due to non-equilibrium conditions (e.g. fast cooling of the sample) during the fabrication.

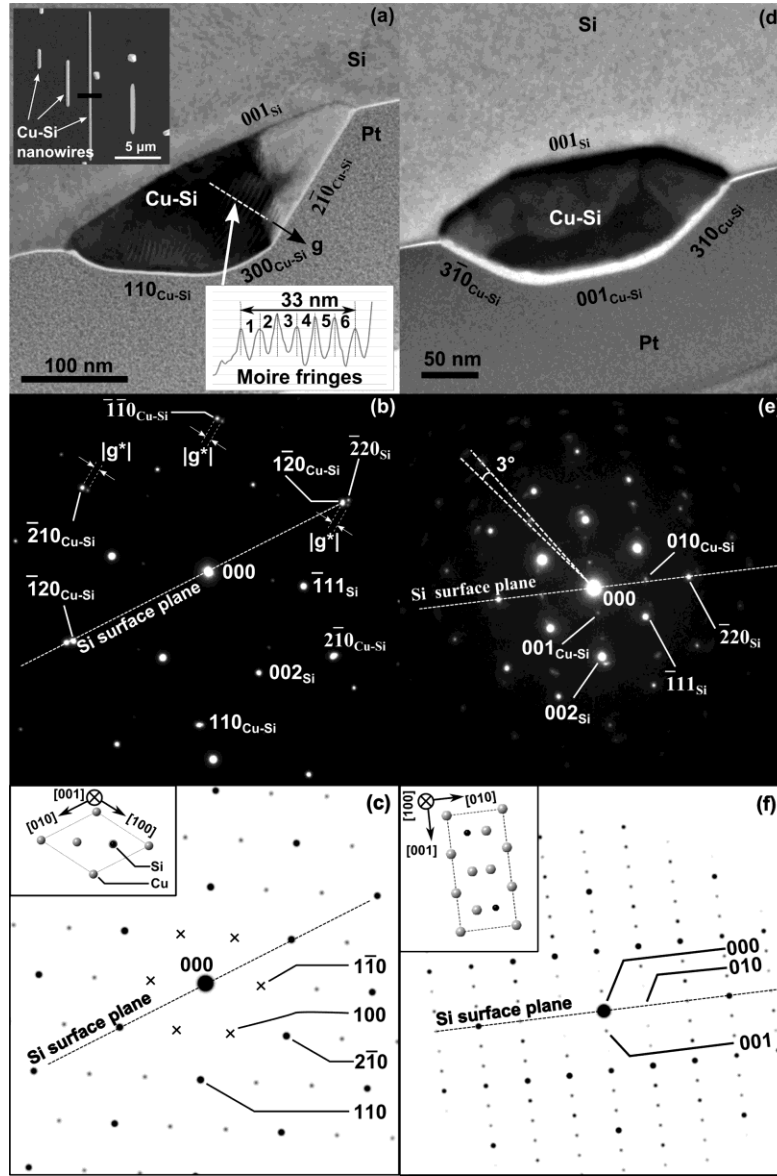
From the TEM micrograph, the nanowire grew slightly into the Si layer with noticeable ‘hut’ shape cross section. The resultant geometry can be explained from its TEM DP, which is shown in Figure 10b. The DP includes Si region, which is projected along the Si[110] direction. The Cu<sub>3</sub>Si DP is comprised of six primary reflections, i.e.  $\bar{1}\bar{1}0_{\text{Cu-Si}}$ ,  $1\bar{2}0_{\text{Cu-Si}}$ ,  $2\bar{1}0_{\text{Cu-Si}}$ ,  $110_{\text{Cu-Si}}$ ,  $\bar{1}20_{\text{Cu-Si}}$ , and  $\bar{2}10_{\text{Cu-Si}}$  ( $\sim 60^\circ$  apart between the two nearest reflections), with a measured g-value of  $0.493 \text{ \AA}^{-1}$  each. These experimental results are in good agreement with those in the simulated patterns in Figure 10c, which was projected



along  $\text{Cu}_3\text{Si}[001]$  direction. The simulated reflections have higher intensities on locations with multiplicities of  $110_{\text{Cu-Si}}$  and  $2\bar{1}0_{\text{Cu-Si}}$  vectors. The former and latter are equivalent with a  $g$ -value of  $0.493 \text{ \AA}^{-1}$ , which is identical to the experimental data. The inset of Figure 10c shows the atomic orientation of the  $\eta\text{-Cu}_3\text{Si}$  structure with the same orientation as the simulated and experimental DP. As can be seen, the nanowire aligned itself such that its Miller index,  $1\bar{2}0_{\text{Cu-Si}}$ , is parallel to the Si surface along the  $\bar{2}20_{\text{Si}}$  direction. However, the two planes did not match exactly and have a  $\sim 6\%$  lattice misfit error (see Appendix I) with a  $< 1^\circ$  tilt. Correlating these reflection indices to the nanowire in Figure 10a, we observed that the top of the nanowire has a  $300_{\text{Cu-Si}}$  facet and the two sides have a  $110_{\text{Cu-Si}}$  facet (equivalent to  $210_{\text{Cu-Si}}$ ). Since a higher Miller index plane grows faster than its lower Miller index counterpart, the nanowire with  $300_{\text{Cu-Si}}$  facet grew faster and resulted in the ‘hut’ shape. Moiré fringes seen in the nanowire (Figure 10a) can be correlated to the additional reflections around  $1\bar{2}0_{\text{Cu-Si}}$ ,  $\bar{1}\bar{1}0_{\text{Cu-Si}}$  and  $\bar{2}10_{\text{Cu-Si}}$ . A white dash line across the Moiré region gives a contrast profile, which is shown in the lower inset of Figure 10a. The period of this pattern was  $33 \text{ nm}/6 \text{ cycles} = 5.5 \text{ nm}$  period or  $\sim 0.018 \text{ \AA}^{-1}$  in  $k$ -space, which agrees well with the measured  $|g^*| \approx 0.018 \text{ \AA}^{-1}$  in the Figure 10b. It may be noted that the projection along  $\text{Cu}_3\text{Si}[\bar{3}\bar{3}1]$  also shows similar DP patterns as in Figure 10b. However,  $\text{Cu}_3\text{Si}[\bar{3}\bar{3}1]$  does not have periodicity with the Si substrate along the growth direction of the nanowire. Therefore, based on the lattice misfit theory,  $\text{Cu}_3\text{Si}[001]$  orientation is a more plausible outcome of this experimental result [102].

A second self assembled Cu-Si nanowire on Si(001) is compared to the first nanowire in Figure 10a-b. It may be noted that the second nanowire was fabricated with the same conditions as the first nanowire. Figure 10d-e show a cross-sectional TEM image and its DP of the second specimen, respectively. The Cu-Si DP consisted of vertical and horizontal reflections with a period of  $\sim 0.14 \text{ \AA}^{-1}$  and  $\sim 0.28 \text{ \AA}^{-1}$  in  $k$ -space, respectively. The DP pattern is quite different from those of that in Figure 10b. To understand this

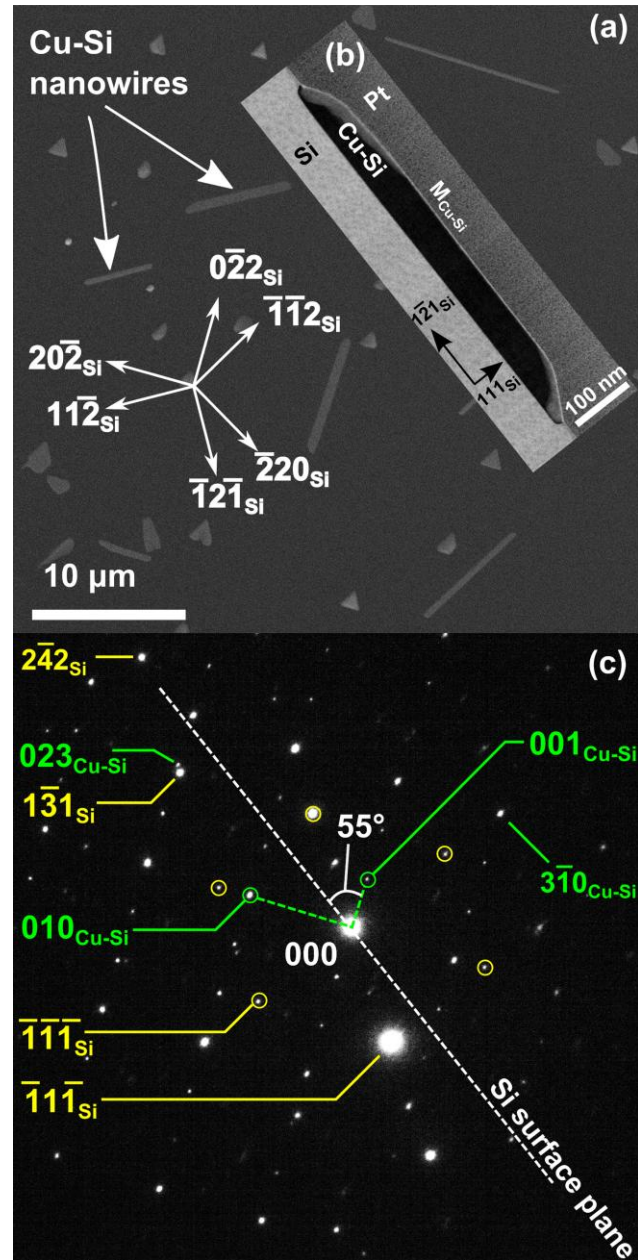
DP, we rotated the  $\eta$ -Cu<sub>3</sub>Si crystal to project along [100] direction (see inset of Figure 10f) that resulted in DP patterns very similar to those in Figure 10e. Hence, the nanowire grew on the substrate with its crystallographic plane, 010<sub>Cu-Si</sub>, and when matched with the Si surface plane,  $2\bar{2}0_{\text{Si}}$ , resulted in -8% lattice misfit error. The Cu<sub>3</sub>Si grains were rotated  $\sim 3^\circ$ , possibly due to the higher lattice misfit (c.f. the prior case in Figure 10a-b) and to relieve the lattice strain. From the DP analysis, the Miller indices can be correlated back to the nanowire in Figure 10d, which shows the top facet has a 001<sub>Cu-Si</sub> plane while the two side facets have {013}<sub>Cu-Si</sub> planes. Because the latter has a higher Miller index value than the former, the two side facets grew faster than the top facet that resulted in a ‘flat top’ shape nanowire. However, the DP interpretation given above for Figure 10e is not unique. If the  $\eta$ -Cu<sub>3</sub>Si was projected along [010] and [110], the simulated DP will give the same results as Cu<sub>3</sub>Si[100] projection. Nonetheless, the three orientations, Cu<sub>3</sub>Si[100], Cu<sub>3</sub>Si[110] and Cu<sub>3</sub>Si[010], will have a 001<sub>Cu-Si</sub> plane as the top facet of the nanowire.



**Figure 10:** Two self assembled Cu-Si nanowires on Si(001) with different crystallography results. Cross section TEM BF images of the first Cu-Si nanowire are shown in (a) while the second nanowire are shown in (d). (b)&(e) Electron DP of Cu-Si nanowires in (a)&(b), respectively, that are supported by simulation results in (c)&(f), respectively, which show the nanowires grew along  $\text{Cu}_3\text{Si}[001]$  &  $\text{Cu}_3\text{Si}[100]$  directions, respectively. Simulations were conducted with CrystalMaker® and SingleCrystal®

### 3.4.2 Self Assembled Cu-Si Nanowires on Si(111)

Self assembled Cu-Si nanowires on Si(111) grew in six different directions (with a  $30^\circ$  angle between the two nearest vectors) as shown in Figure 11a. The long axis direction of the nanowires can be determined from the cross-sectional TEM sample (see Figure 11b). The resultant DP is shown in Figure 11c, which consisted of both the Cu-Si and Si layers. The Si zone axis is along  $[10\bar{1}]$  direction, which is a family of  $[110]$ . The right angle of the nanowire, as can be seen, is parallel to  $2\bar{4}_2\text{Si}$  or the  $\langle 112 \rangle$  direction, which is also parallel to the Si surface. Since  $[110]$  and  $[112]$  are  $15^\circ$  apart, the Cu-Si nanowires in this case grew parallel to the families of  $\langle 110 \rangle$  and  $\langle 112 \rangle$  directions. The Cu-Si DP has very similar patterns and g-values as that of those projected along  $\text{Cu}_3\text{Si}[100]$  (see Figure 10f), suggesting the presence of a  $\eta\text{-Cu}_3\text{Si}$  structure. An XEDS evaluation of the nanowire shows an atomic ratio of 3 to 1 for Cu and Si elements, respectively, supporting the  $\eta\text{-Cu}_3\text{Si}$  structure observation. However, the  $001_{\text{Cu-Si}}$  grain was tilted  $55^\circ$  from the Si surface plane, forming asymmetrical planes with the Si surface. As a result, a matching lattice plane between the Cu-Si and Si surface cannot be seen in the DP, albeit it may occur at higher indices. Nevertheless, the nearest two grains observed in the DP were those of  $1\bar{3}1_{\text{Si}}$  plane with a d-value of  $1.637 \text{ \AA}$  and  $023_{\text{Cu-Si}}$  plane with a d-value of  $1.709 \text{ \AA}$  as shown in Figure 11c, while rotated  $10^\circ$  from each other. This resulted in a lattice misfit error of about 4%. Therefore, the nanowire may grow such that its crystal orientation matched the  $1\bar{3}1_{\text{Si}}$  index. From the DP, the top facet of the nanowire is along the  $3\bar{1}0_{\text{Cu-Si}}$  plane. Likewise for the nanowire in Figure 11d, in addition to  $\text{Cu}_3\text{Si}[001]$ , the long axis orientation of the nanowire could be projected along the  $\text{Cu}_3\text{Si}[010]$  or  $\text{Cu}_3\text{Si}[110]$  direction.



**Figure 11:** (a) A typical SEM image of self assembled Cu-Si nanowires on Si(111). (b) A cross sectional TEM view of a Cu-Si nanowire on Si(111). (c) Electron DP of the TEM specimen in (b). The vector normal to the nanowire surface is  $\text{Cu}_3\text{Si}[3\bar{1}0]$ .

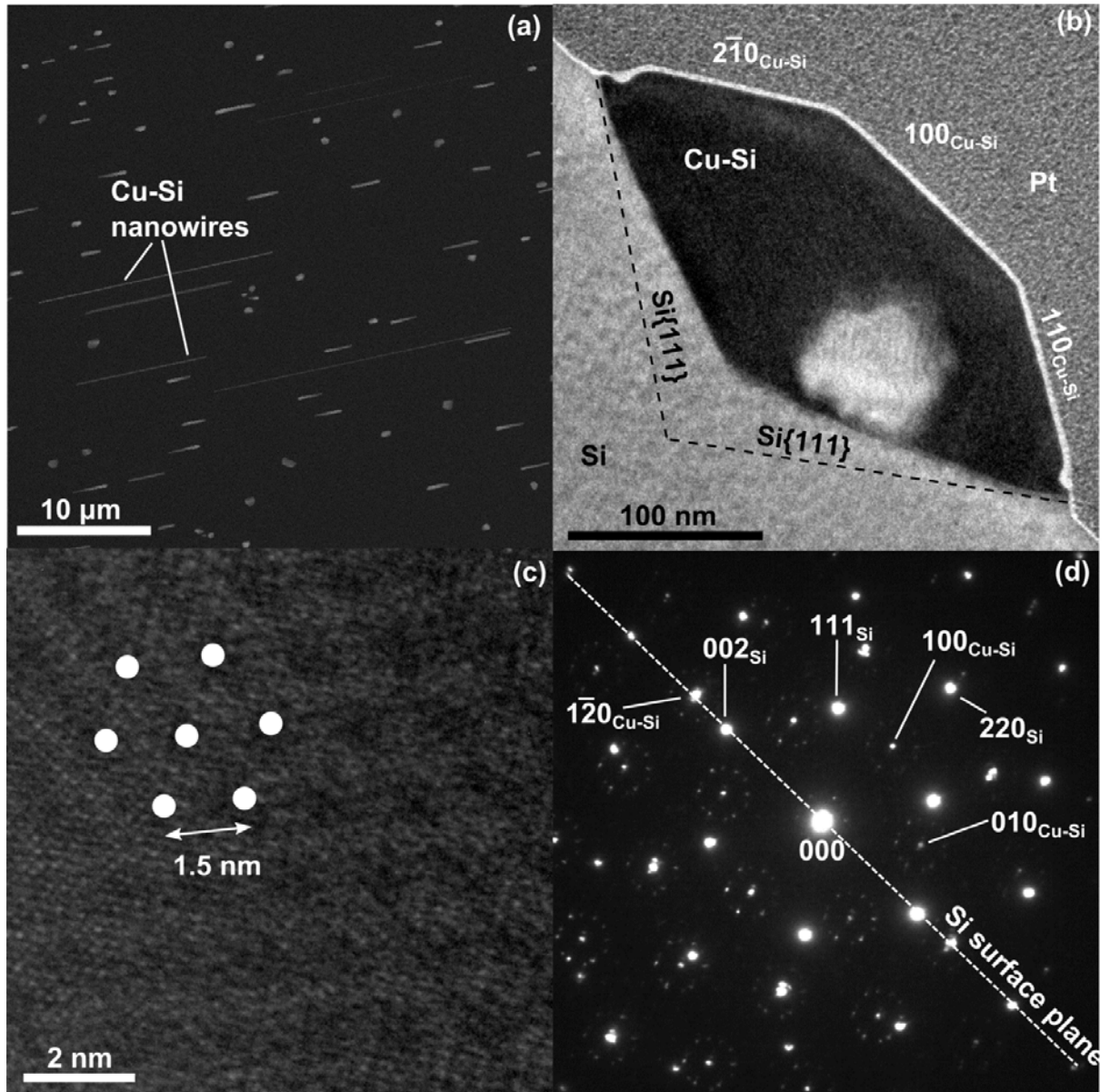
### 3.4.3 Self Assembled Cu-Si Nanowires on Si(110)

Typically, self assembled Cu-Si nanowires on Si(110) grow in parallel directions, as shown in Figure 12a. A cross-sectional TEM image of a nanowire forming a shallow ‘V’ interface with the substrate is shown in Figure 12b and its DP is shown in Figure 12d. The DP from the Si layer is also shown in Figure 12d and shows a  $\text{Si}[\bar{1}10]$  zone axis. The  $\text{Cu}_3\text{Si}$  DP has nearly identical positions and g-values ( $0.28 \text{ \AA}^{-1}$ ) as the simulated reflections in Figure 10c. Therefore the nanowire possessed  $\eta\text{-Cu}_3\text{Si}$  phase and longitudinally projected along the  $\eta\text{-Cu}_3\text{Si}[001]$  direction. We verified that the nanowire was indeed a  $\text{Cu}_3\text{Si}$  via XEDS measurement. From the simulation in Figure 10c, we can infer that the  $\text{Cu}_3\text{Si}$  DP has six primitive vectors with an equivalent g-value, in which two of the vectors are  $010_{\text{Cu-Si}}$  and  $100_{\text{Cu-Si}}$ . However, these primitive vectors are not visible in the simulation and therefore marked with an ‘x’. The crystallographic orientation of the nanowire was such that the top facet was  $100_{\text{Cu-Si}}$ , while the two side facets had  $210_{\text{Cu-Si}}$  and  $110_{\text{Cu-Si}}$  planes, which both have equal g-values of  $0.493 \text{ \AA}^{-1}$  (c.f. Figure 12b and 10c). The ‘V’ interface of the nanowire possessed  $\bar{2}\bar{1}0_{\text{Cu-Si}}$  and  $\bar{3}10_{\text{Cu-Si}}$  planes with an equal g-value of  $0.75 \text{ \AA}^{-1}$ , respectively. As can be seen in Figure 12d, the nanowire grew such that the  $\bar{1}20_{\text{Cu-Si}}$  grain was parallel to the  $002_{\text{Si}}$  grain, whereby the two grains have -25% lattice misfit error. The error is unusually large for a self assembly process according to equilibrium theory of lattice misfit (see section 8.3.1 of Reference [103] and Reference [102]). Therefore other factors may contribute to the growth mechanics. From the  $\text{Cu}_3\text{Si}$  DP, it can be seen that each grain has a double diffraction with a radius or g-value of  $\sim 0.13 \text{ \AA}^{-1}$ . We can correlate the double diffractions to the Moiré fringes in Figure 12c, which is a TEM image of a small region in the right hand side of the nanowire. The Moiré patterns formed vague hexagonal spots with a d-spacing of  $\sim 1.5 \text{ nm}$ , which translates to  $0.067 \text{ \AA}^{-1}$  in k-space. Therefore, the period of the Moiré hexagonal spots is consistent with the radius of the double diffractions. The intensities of the simulated reflections are not consistent with the experimental observations. This

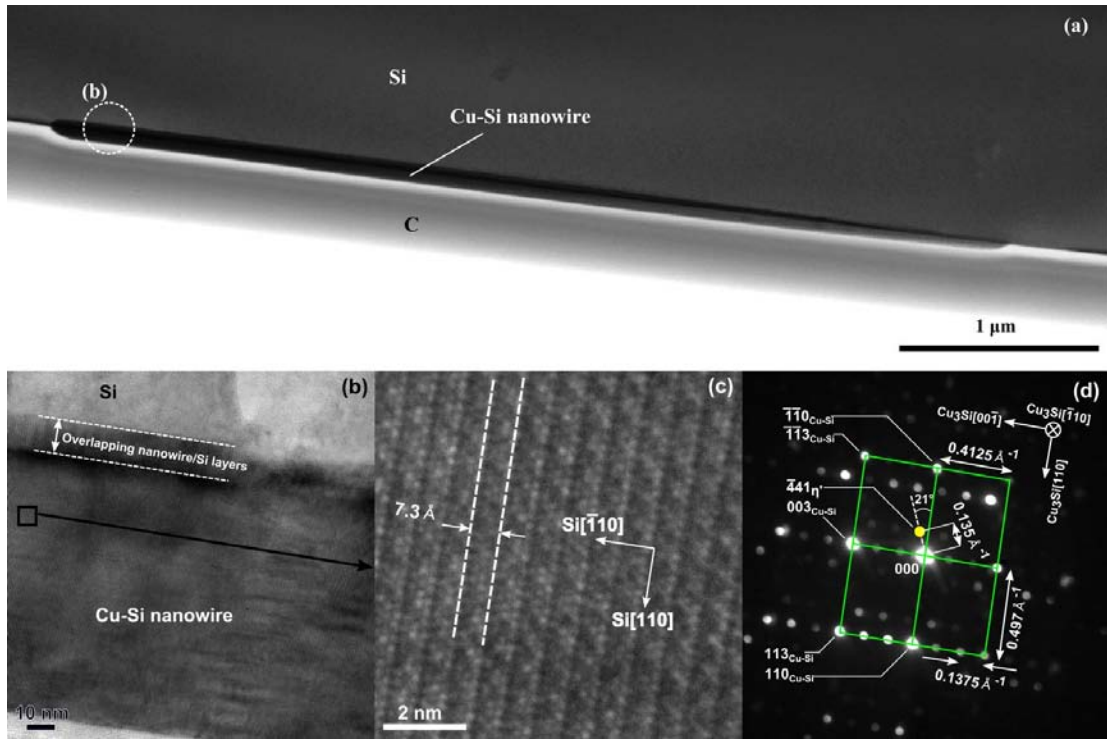
phenomenon could be either due to a different crystal stacking order (which would result in different structure factors) or double diffraction from a thick specimen. In order to resolve this, we performed another TEM experiment on a second nanowire that was cut along longitudinal direction, as shown in Figure 13a. From the figure, a white dashed circle indicates an area of the nanowire where a HRTEM image was obtained (see Figure 13b). In the cross section specimen on Si(110), the nanowire formed a shallow ‘V’ interface on the Si substrate. Therefore, when observed from a longitudinal cut perspective as in Figure 13b, the ‘V’ interface may cause overlapping areas of the nanowire and Si substrate. Periodic lines within the nanowire can be seen. For a further inspection, a small area of the nanowire was further enlarged and shown in Figure 13c. Parallel lines seen in the TEM figure formed a prominent  $\sim 7.3$  Å periodicity that indicates the presence of  $\eta$ -Cu<sub>3</sub>Si with Cu<sub>3</sub>Si[001] axis parallel to the longitudinal direction of the nanowire. It may be noted that the Si zone axis of this specimen is not shown in the report but was determined to be along the Si[00 $\bar{1}$ ] direction. The periodicity in Figure 13c can be further analyzed with DP of the specimen. In this case, we used the convergent beam electron diffraction (CBED) technique due to small dimension of Cu<sub>3</sub>Si region (<100 nm). The resulting CBED is shown in Figure 13d, and strongly agrees with the simulation when the crystal is projected along the Cu<sub>3</sub>Si[120] direction. The longitudinal direction of the nanowire is along Cu<sub>3</sub>Si[001], conforming to the results observed in the cross-sectional TEM specimen in Figure 12. However, the top facet of this nanowire is along the {110}<sub>Cu-Si</sub> planes as opposed to the {100}<sub>Cu-Si</sub> planes found in Figure 12, where the two vectors are rotated by 30°. The green boxes in the figure outline the  $\eta$ -Cu<sub>3</sub>Si reflections forming parallel streaks on locations  $11w_{\text{Cu-Si}}$ ,  $00w_{\text{Cu-Si}}$ ,  $11w_{\text{Cu-Si}}$ , etc., where  $w$  is an integer. A single unit of  $w$  was measured as  $0.1375 \text{ Å}^{-1}$ , which is consistent with the 7.3 Å period observed in Figure 13c. One of the Cu<sub>3</sub>Si reflections not observed in the  $\eta$ -Cu<sub>3</sub>Si TEM simulation is indicated with a yellow dot. The reflection has an approximately 0.35 of [001]<sub>Cu-Si</sub> and 0.25 of [ $\bar{1}\bar{1}0$ ]<sub>Cu-Si</sub> distances, which highly suggests superlattice structures due to a  $\eta'$ -Cu<sub>3</sub>Si

phase and as such the index is labeled as  $\bar{4}41$  following the notations used by Wen *et al.* in Reference [98]. Therefore, the TEM specimen from this longitudinal cut nanowire consisted of  $\eta$ -Cu<sub>3</sub>Si and  $\eta'$ -Cu<sub>3</sub>Si structures. The latter may explain the discrepancy in DP intensities between the simulated reflections in Figure 10c and the experimental data in Figure 12c, although further studies are needed for verification.





**Figure 12:** (a) A typical SEM view of self assembled Cu-Si nanowires on Si(110). (b) A cross sectional TEM specimen of a Cu-Si nanowire that shows a shallow ‘V’ interface with the Si substrate. (c) Moiré patterns in the nanowire. The image was obtained and magnified at the right hand corner of the nanowire in (b). (d) Electron DP of the specimen in (b). The nanowire grew along  $\text{Cu}_3\text{Si}[001]$  direction.



**Figure 13** (a) Longitudinal cut TEM specimen of a self assembled Cu-Si nanowire on Si(110). (b) A magnified TEM image of an area within the dotted circle shown in (a). (c) A HRTEM image of the nanowire shows a 7.3 Å period. (d) Electron DP of the TEM specimen shows a mixture of  $\eta$  and  $\eta'$  phase.

### 3.5 Summary

The material composition and crystallographic directions of Cu-Si nanowires was studied in detail. XEDS data show that  $\text{Cu}_3\text{Si}$  was the main phase detected in the Cu-Si nanowires on Si(001), Si(110), and Si(111). The crystallographic orientation of self-assembled Cu-Si nanowires with respect to Si(001), Si(110), and Si(111) substrates was studied using electron diffraction patterns. The results indicate a sharp Cu-Si/Si boundary, which suggests low Cu contamination in neighboring regions. On each Si substrate, the nanowires formed a different heteroepitaxy resulting in different crystallographic orientation, i.e Cu-Si nanowires on Si(001) grew along  $\eta\text{-Cu}_3\text{Si}[001]$  and  $\eta\text{-Cu}_3\text{Si}[100]$ , Cu-Si nanowires on Si(111)  $\eta\text{-Cu}_3\text{Si}[100]$ , and Cu-Si nanowires on Si(110) grew along  $\eta\text{-Cu}_3\text{Si}[001]$ . The two Cu-Si nanowires on the same Si(001) substrate with different crystallographic orientations suggest a metastable condition in the growth mechanics on Si(001). From our TEM specimens, crystal twinning was not observed and all the nanowires have clear and smooth facets.

## 4. MATERIAL CHARACTERIZATION OF THE ELECTRICAL PROPERTIES OF SELF ASSEMBLED CU-SI NANOSTRUCTURES

### 4.1. Introduction

Most studies on electrical properties of Cu-Si were performed on thin film, e.g. see References [52, 59, 104]. Comparatively, very few electrical resistivity studies have been conducted on Cu-Si nanowires or nanostructures. Jung and *et al.* in Reference[60] have recently published the measured electrical resistivity of a free standing self assembled Cu<sub>3</sub>Si nanowire. The authors performed a four point probe measurement on a 1.78  $\mu\text{m}$  long  $\times$  305 nm diameter nanowire with a resistivity of 21-23  $\mu\Omega\cdot\text{cm}$ . However, the characterization was *ex situ*. Furthermore the Cu-Si nanowires fabricated by Jung *et al.* were free standing and not horizontally on Si(111). Chiu *et al.* in Reference [105] fabricated a smaller  $\eta$ -Cu<sub>3</sub>Si nanowire by solid state reaction between a single crystalline Si nanowire ( $\sim 80$  nm diameter) and Cu pads. The resultant Cu-Si nanowire grew about 1.4 times larger in diameter with a resistivity of 206  $\mu\Omega\cdot\text{cm}$ . However, Chiu *et al.* employed a two point probe method for the resistivity measurement. Therefore, contact resistances were included and the actual resistivity of the nanowire is not known. Smaller Cu-Si nanostructures were electrically characterized as reported by Dimitri *et al.* in Reference [106]. The authors fabricated self assembled Cu<sub>2</sub>Si on Si(111) with a resistivity of  $\sim 8$   $\mu\Omega\cdot\text{cm}$  using an *in situ* square point probe method via scanning tunneling microscopy (STM). However, the Cu<sub>2</sub>Si nanostructures studied in Reference [106] were a submonolayer of Cu clusters [107-109]. Thus, those nanostructures were not truly Cu-Si and may not reflect the properties of metal silicides.

The goal of this chapter is to study electrical properties of Cu-Si nanowires on Si from dimensions greater than 100 nm to below 10 nm. The electrical resistivity was measured on the Cu-Si nanowires with dimensions  $>100\text{nm}$  using a four point probe method. To characterize the failure current

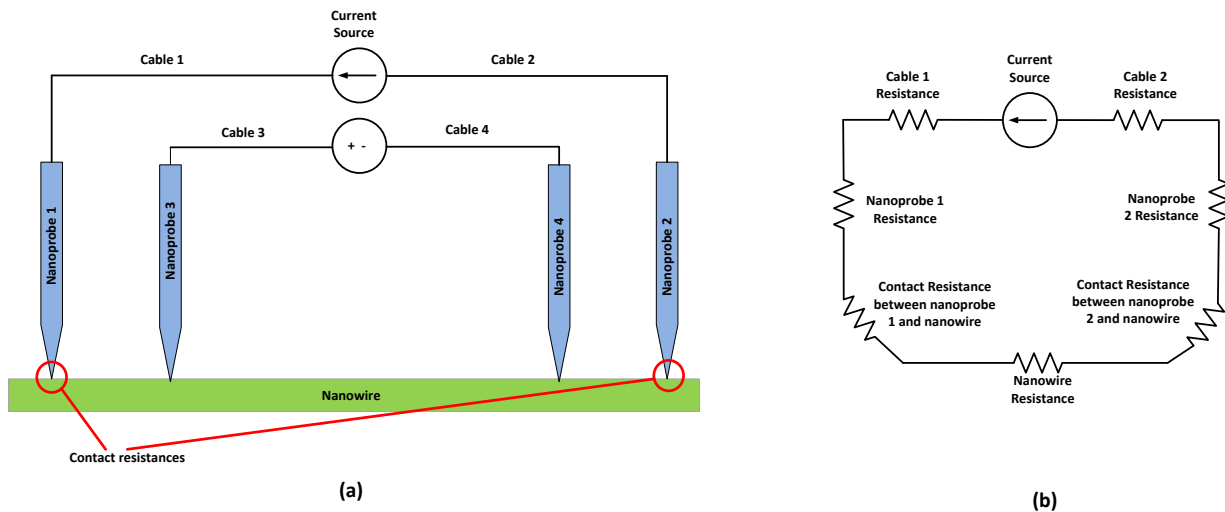
density, the Cu-Si nanowires were electrically stressed until the wire broke. In these resistivity and electrical failure studies, two or four nanoprobe were employed. To characterize sub 10 nm nanostructure, scanning tunneling microscopy (STM) was used to obtain I-V and  $dI/dV$  spectroscopy measurements.

## **4.2 Experimental Procedures**

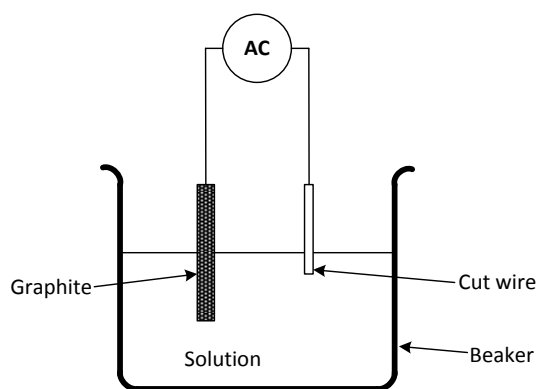
### **4.2.1 Electrical Resistivity Measurement with a Four Point Probe Method**

The main advantage of using a four point probe method to measure electrical resistivity is to reduce the effects of parasitic resistances, which are not components of the Cu-Si nanostructure. A typical four point probe setup is shown in Figure 14, which has a pair of nanoprobe (1 & 2) for sourcing current,  $I$ , and another pair nanoprobe (3 & 4) for sensing voltage,  $V$ . Thus, the resistance,  $R$ , is computed with the slope of the measured  $V$  vs.  $I$  curves. Consider the loop around the current source in Figure 14a, which can be modeled as a distributed circuit (see Figure 14b). Due to high current, significant voltage will drop across the parasitic components, i.e. cables, nanoprobe, and contact resistances. Therefore, to avoid measuring these parasitic effects, another pair of nanoprobe for sensing a voltage is used and placed between the current source probe on the nanowire.

The nanoprobe in this experiment were prepared by electrochemically etched platinum-iridium (Pt/Ir) and tungsten (W) tips, which were prior cut to  $\sim 10$ - $12$  mm long from a spool of wire. A simple setup for etching these tips is shown in Figure 15. The solution to etch Pt-Ir tips was 1.5 molar calcium chloride ( $\text{CaCl}_2$ ) while to etch W tips was 2 molar sodium peroxide ( $\text{NaOH}$ ). The procedures to etch the Pt-Ir and W tips are different. In the Center for Nanoscale Materials (CNM) at Argonne National Lab (ANL), the following procedures are used. Pt-Ir tips were etched at  $35 V_{ac}$  for 90 seconds, then at  $30 V_{ac}$  for 45 seconds and finally at  $28 V_{ac}$  until the etching stopped. W tips were etched at  $5 V_{ac}$  until the process stopped.



**Figure 14:** (a) A four point probe method setup to measure electrical resistivity of Cu-Si nanowires. (b) A distributed circuit of (a) with some non-trivial parasitic resistances across the current loop.



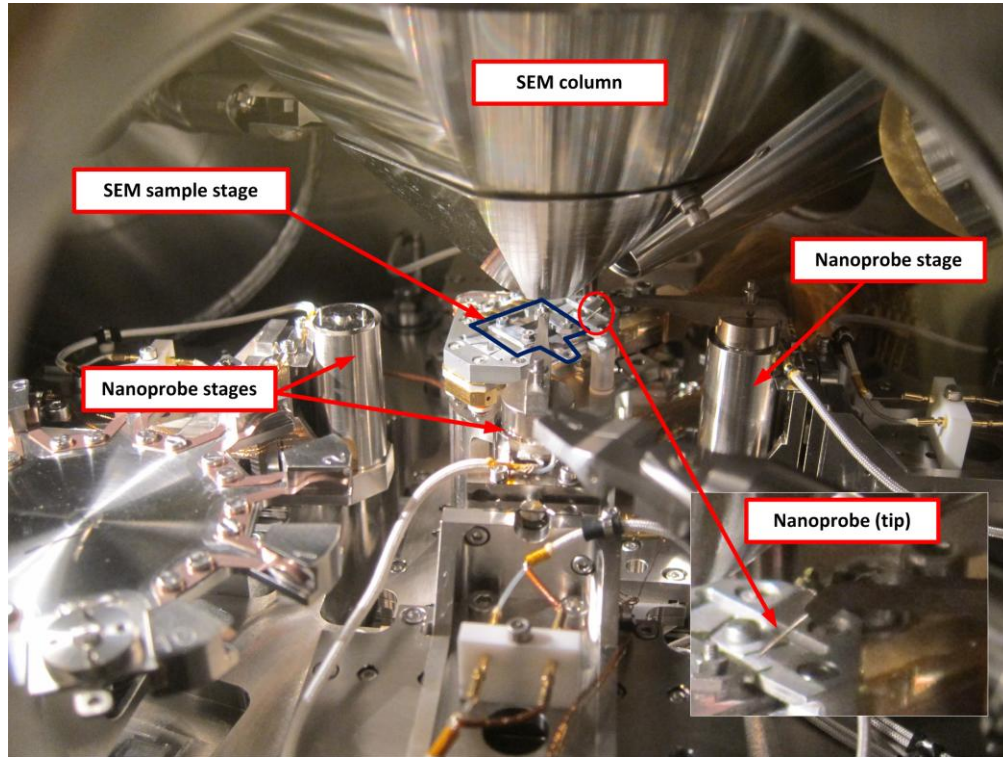
**Figure 15:** A simplified schematic of electrochemical etch of nanoprobe tips. For Pt-Ir tips, the solution was 1.5 M  $\text{CaCl}_2$  whereas for W tips, the solution was 2M NaOH. The two different tips will need a different AC voltages ( $V_{ac}$ ) for etching as given in the text above.

Referring to Figure 16, the prepared tips were inserted into tip holders (see inset), which were then mounted onto the four nanoprobe stages under the SEM column in the Omicron system (see Chapter 2.3). Each nanoprobe stage can hold a tip (nanoprobe), which can independently move in x-y-z direction via piezoelectronic transducers (or controllers) to bring the tips in to physical contact with a nanostructure.

Because the four point stages are in the same UHV system as the e-beam evaporator, *in situ* electrical resistivity measurements were performed, which preserved the pristine condition of the self assembled Cu-Si nanowires. In this thesis, resistivity of self assembled Cu-Si nanowires on Si(111) and Si(110) were *in situ* measured with the four point probe method. A Keithley model 6430 current source was used to sweep electrical current from -10  $\mu\text{A}$  to 10  $\mu\text{A}$  and back to -10  $\mu\text{A}$  in a 1  $\mu\text{A}$  step. Each step has a wait time of 0.3 sec. A shorter wait time would result in a dc current error between the upward and downward scans. This may be due to stored electrical charges residing within the system under test. The voltage was recorded by Keithley model 2182A. The resistance value,  $R$ , computed from the Keithley data needs to be converted to resistivity,  $\rho$ , with the following formula:

$$\rho = \frac{RA}{L} \text{ } [\mu\Omega.\text{cm}] \quad (4)$$

where,  $L$  is the distance between the two voltage nanoprobe in cm and  $A$  is the cross section area of the nanowire in  $\text{cm}^2$ . The latter can be computed from a cross section TEM micrograph of a nanowire via imageJ software [110].



**Figure 16:** A picture of the analysis-chamber in the Omicron Nanotechnology System at the CNM at ANL. A sample with nanowires will be mounted on a Mo holder (blue outline), which in turn will be inserted into the SEM sample stage underneath the SEM column. The SEM stage is surrounded by four nanoprobe stages for either electrical resistivity measurement or (low resolution) STM. An enlarged image at the lower right corner shows a nanoprobe (tip).

#### 4.2.2 Electrical Current Failure with a Two Point Probe Method

In this experiment, nanowires were electrically stressed until a failure occurred, which is defined in this thesis as an open circuit. Since the current failure experiment is destructive, resistivity measurement (if needed) must be performed first. During the current stressing, an electrical current is



sourced to the nanowire and ramped from 0 to 100 mA (assuming most nanowires will fail before this value) at 5  $\mu\text{A/s}$ . A two point probe method was used for this electrical stressing experiment because surface contact from the voltage probes can modify the outcome. This is because probe contact can artificially induced surface defects on Cu-Si nanowires resulting in an accelerated failure. Hence, a two point probe method was employed here. The setup for the two-point probe method was very similar to that of a four point probe except the voltage sensing is done internally by the Keithley instruments.

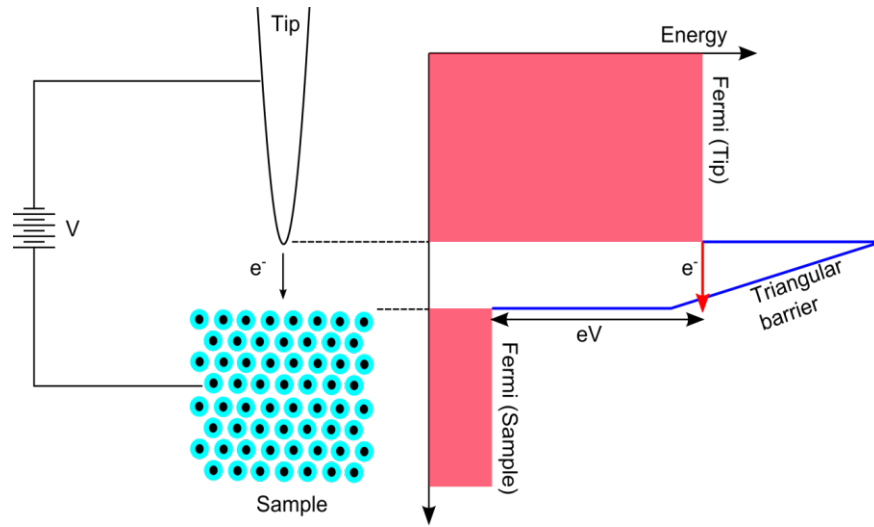
#### 4.2.3 Electrical Spectroscopy with STM

Although a scanning tunneling microscopy (STM) is a surface analytical tool, it can be used for electrical characterization by performing I-V and  $dI/dV$  spectroscopy. The STM used in this chapter was a variable-temperature (VT) UHV scanning probe microscopy located at CNM, ANL, IL. An e-beam evaporator is also connected to the UHV system. Therefore, samples were transferred from the e-beam evaporator to the STM system without breaking the UHV. In doing so, samples analyzed by the STM are considered pristine and *in situ*.

A basic operation of a STM is illustrated in Figure 17, which shows a tip, a sample (substrate), and a voltage power supply,  $V_{\text{bias}}$ . When there is a differential voltage ( $V_{\text{bias}}$ ) between the tip and the sample, the energy barrier between them will form a triangular shape. If the tip gradually approaches the sample, electrons will tunnel across the triangular barrier [111]. The tunneling current,  $I$ , and set point voltage,  $V_{\text{bias}}$ , are converted to I-V and  $dI/dV$  data.

Conventionally,  $V_{\text{bias}}$  refers to the sample (substrate) voltage. If  $V_{\text{bias}}$  is positive, electrons will tunnel from the tip to the empty electronic states of the sample. If  $V_{\text{bias}}$  is negative, the electrons will tunnel from the filled electronic states of the sample to the tip. By moving the tip across an area of the sample, a surface image can be constructed from the electron tunneling data based on either empty or

filled electronic states. From the same tunneling data, I-V and  $dI/dV$  curves can be plotted on a local surface. It may be noted that the local density of states (LDOS) of a surface is proportional to the differential conductance ( $dI/dV$ ) [111]. Both I- V and  $dI/dV$  data were obtained from self assembled Cu-Si nanoislands on Si(110).

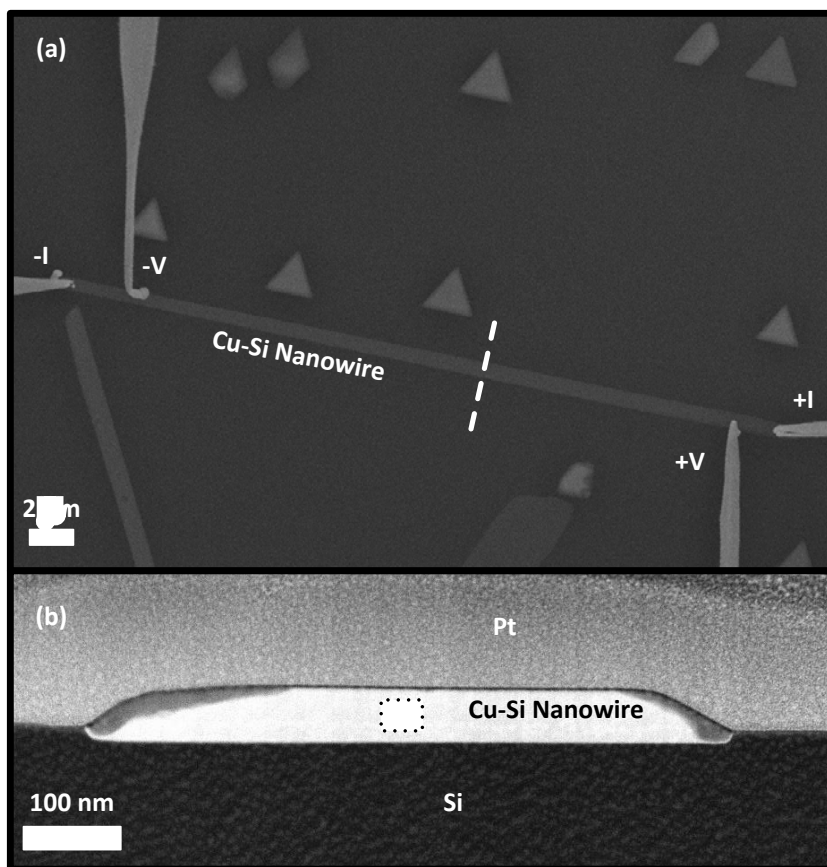


**Figure 17:** A simplified schematic of a STM operation. The figure shows a bias voltage,  $V$ , is applied between a nanoscale tip and a sample. When the tip and the sample is closed enough, electrons will begin tunneling across the energy barrier between them, which can be approximated with a triangular shape [111].

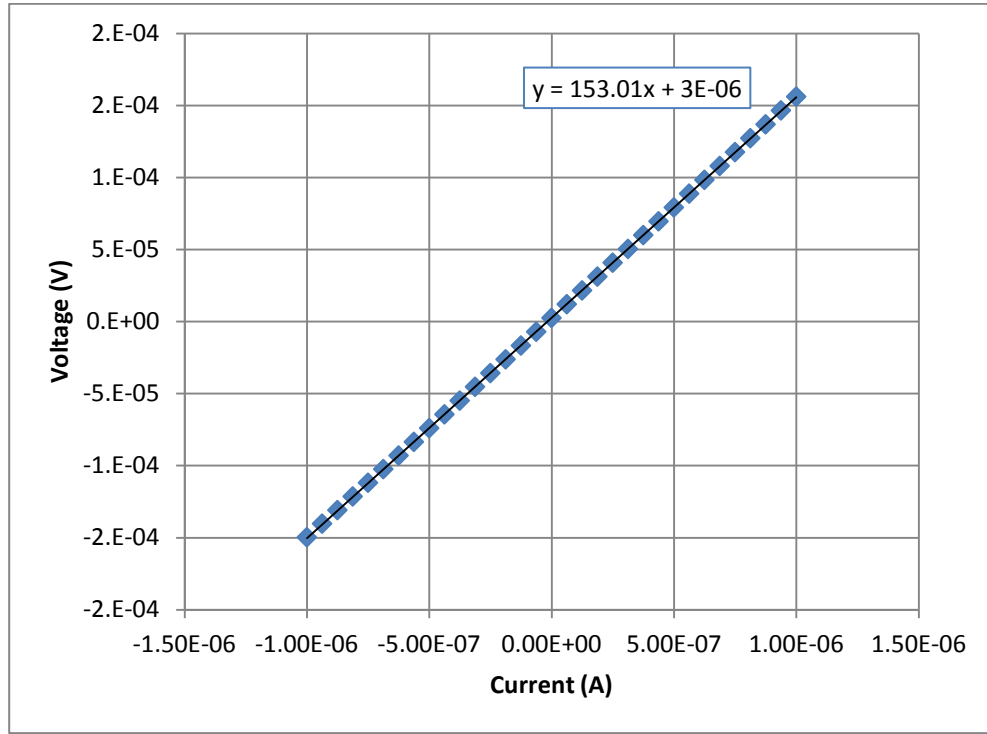
### 4.3 Electrical Characterization Results and Discussion

#### 4.3.1 Electrical Resistivity of Cu-Si Nanowires on Si(111)

A Cu-Si nanowire with 662 nm width was selected for electrical characterization, which is denoted as nanowire X1. This was a typical self assembled Cu-Si nanowire on Si(111) with dimensions of hundreds of nm in width and 10-20  $\mu\text{m}$  long. Shown in Figure 18(a) is an example of how an *in situ* four point probe setup on nanowire X1 was performed here and throughout the thesis. The outer two probes, denoted as +I and -I, were the current source, while the inner two probes, denoted as +V and -V, were used to measure the voltage. The distance between the two voltage probes is denoted as L. The I-V data were then plotted, which is shown from one of the results ( $L = 7.8 \mu\text{m}$ ) in Figure 19. The I-V plot is linear and Ohmic in characteristics, which shows that X1 behaves as metallic. The resistance,  $R = 153 \Omega$ , of this plot is obtained from the linear fitted slope. To improve the accuracy of R, six set of I-V data were obtained and on three different L spacing. Thus, a total of 18 sets of I-V data were used to calculate the resistivity of nanowire X1. To compute the resistivity, we need the cross section area, which was obtained from TEM image shown in Figure 18(b) that averages  $31,371 \text{ nm}^2$ . Using equation 4.1, the resistivity,  $\rho$  of nanowire X1 is  $45.59 \mu\Omega\cdot\text{cm}$ . A summary of the results and physical dimensions of nanowire X1 are shown in Table I.



**Figure 18:** (a) A SEM image of an *in situ* four point probe resistivity measurement of a Cu-Si nanowire X1 on Si(111) with a dashed line representing the FIB location for TEM analysis. (b) A cross section TEM image of the nanowire X1 with a dotted rectangular indicates XEDS area for material composition verification.



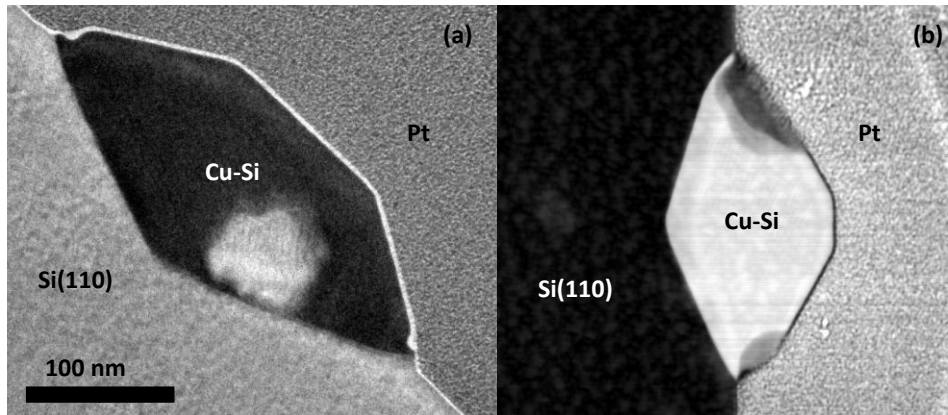
**Figure 19:** Resistance value extrapolated from the linear regression fitting of experimental I-V points of nanowire X1. The slope in the regression equation gives the resistance value of the nanowire in  $k\Omega$ .

**Table I:** Resistance and resistivity of a Cu-Si Nanowire on Si(111)

	Nanowire X1
A ( $\text{nm}^2$ )	$31,371 \pm 1,043$
R ( $\Omega$ ) at 1 <sup>st</sup> L ( $\mu\text{m}$ )	$127.90 \pm 0.05 \Omega$ at $7.79 \pm 0.56 \mu\text{m}$
R ( $\Omega$ ) at 2 <sup>nd</sup> L ( $\mu\text{m}$ )	$226.53 \pm 0.13 \Omega$ at $16.18 \pm 0.54 \mu\text{m}$
R ( $\Omega$ ) at 3 <sup>rd</sup> L ( $\mu\text{m}$ )	$330.09 \pm 0.20 \Omega$ at $25.07 \pm 0.51 \mu\text{m}$
$\rho$ ( $\mu\Omega \cdot \text{cm}$ )	$45.59 \pm 2.07$

#### 4.3.2 Electrical Resistivity of Cu-Si Nanowires on Si(110)

As seen in the previous section, the Cu-Si nanowires on Si(111) were relatively large with widths as large as 1  $\mu\text{m}$ . On the other hand, self assembled nanowires on Si(110) were found to have much smaller widths, e.g. 100-200 nm range. Therefore, resistivity characterization of smaller Cu-Si nanowires were performed on a Si(110) sample. The procedure to fabricate these Cu-Si nanowires on Si(110) was the same as before (see Chapter 2). Two Cu-Si nanowires with  $\sim 320$  nm (denoted as X2) and  $\sim 226$  nm wide (denoted as X3) were selected for *in situ* electrical resistance measurement with a four point probe method. The cross section areas of the two nanowires were  $27,988 \text{ nm}^2$  and  $15,629 \text{ nm}^2$ , respectively, are measured from the cross-sections shown in Figure 20. The resistivity for nanowires X2 and X3 were  $40.2 \pm 1.8 \mu\Omega\cdot\text{cm}$  and  $32.8 \pm 2.3 \mu\Omega\cdot\text{cm}$ , respectively, and computed from their physical attributes listed in Table II.



**Figure 20:** Cross section TEM micrographs of nanowires (a) X1 and (b) X2.

(a) TEM BF image and (b) DF image.

**Table II:** Resistance and resistivity of Cu-Si nanowires on Si(110)

	Nanowire X2	Nanowire X3
A (nm <sup>2</sup> )	27,988 ± 466	15,629 ± 206
R (Ω) at 1 <sup>st</sup> L (μm)	154.26±0.64 Ω at 10.84 ± 0.46 μm	168.75±0.29Ω at 7.82 ± 0.54 μm
R (Ω) at 2 <sup>nd</sup> L (μm)	329.32±0.10 Ω at 23.18 ± 0.43 μm	340.47±0.05 Ω at 16.20 ± 0.61 μm
R (Ω) at 3 <sup>rd</sup> L (μm)	502.62±0.23 Ω at 34.25 ± 0.48 μm	510.89±3.14 Ω at 25.02 ± 0.52 μm
ρ (μΩ•cm)	40.2± 1.8	32.8± 2.3

#### 4.3.3 Electrical Current Stressing of Cu-Si Nanowires

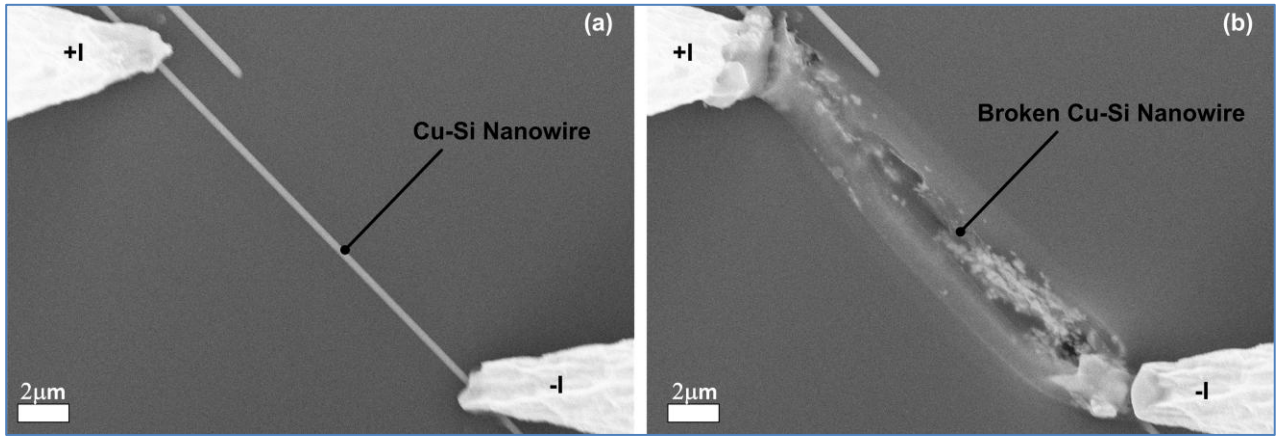
Electrical failure due to current stressing is a fundamental concern in nanowires applications [80]. As such, it is imperative to understand the electrical current limits in a nanowire for designing a reliable system. Thus, nanowire failure from electrical current stressing is commonly studied. Most of these studies have been performed on top-down fabricated nanowires [80]. However, the top-down approach usually produces polycrystalline nanowires. As seen in Chapter 3, the self assembled Cu-Si nanowires were single crystalline and it is expected that single crystalline nanowire to have a higher tolerance against electrical current stress [112]. However, there is a serious lack of studies on failure current density on Cu-Si nanowires. Therefore in this section, failure current density on Cu-Si nanowires was investigated with two different test conditions: (1) failure current density versus nanowire length and (2) failure current density versus nanowire cross section area.

One of the problems stated in Chapter 2 was the lack of direct control of the self assembled nanowires. As a result, the self assembled Cu-Si nanowires have different shapes and sizes. Therefore,

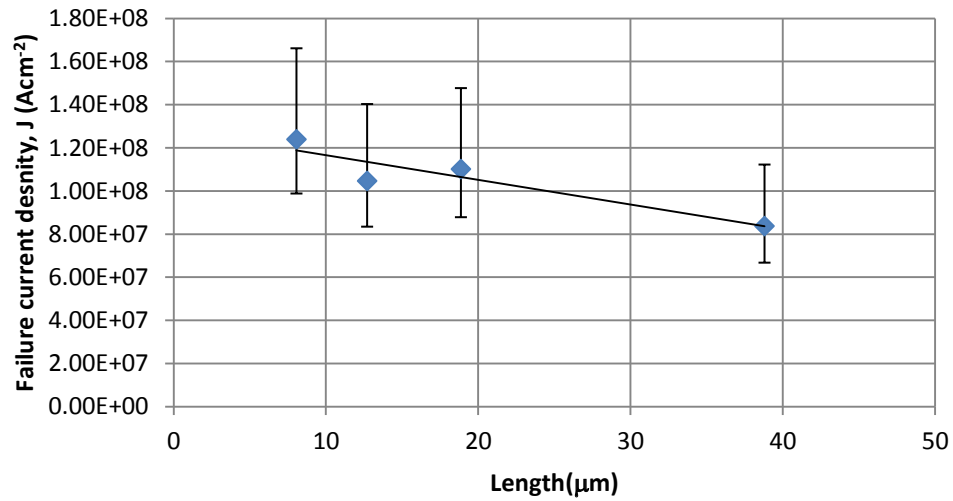
electrical stress experiments required that the nanowire must be very long to have repeatable test conditions when measuring the failure with a constant cross section area. Therefore, the experiments were conducted on Cu-Si nanowires self assembled on Si(110), which can grow up to 200  $\mu\text{m}$  long on the substrate. Thus, a very long  $\sim 200 \mu\text{m}$  (and 305 nm wide) nanowire was selected for the study.

A gradually increasing (at 5  $\mu\text{A/s}$ ) electrical current was delivered to the nanowire via a two point probe method until the nanowire broke (open circuit), see for example in Figure 21. Due to the destructive method in FIB preparation, a cross section TEM micrograph of the nanowire was not obtained. Instead, the cross section area was estimated using methods described in Appendix II. Therefore the failure current density,  $J$  ( $\text{A.cm}^{-2}$ ), was computed based on this estimation. The result of the analysis was plotted in Figure 22, which shows a downward trend. This is a reasonable observation since a longer nanowire will thermally heat up faster and fail quicker [80]. However, due to the large error bars, the type of downward trend (e.g. exponential, linear, etc.) is unclear. In order to make this analysis more accurate, a longer nanowire is needed to produce more data points from a single nanowire. Nonetheless, finding a nanowire of  $>200 \mu\text{m}$  will be very challenging. Another method to reduce uncertainties is to constantly replace worn out nanoprobe tips so that the tips remain sharp most of the time. However, in this failure current density test, this would be prohibitive since it would require new tips for every measurement.



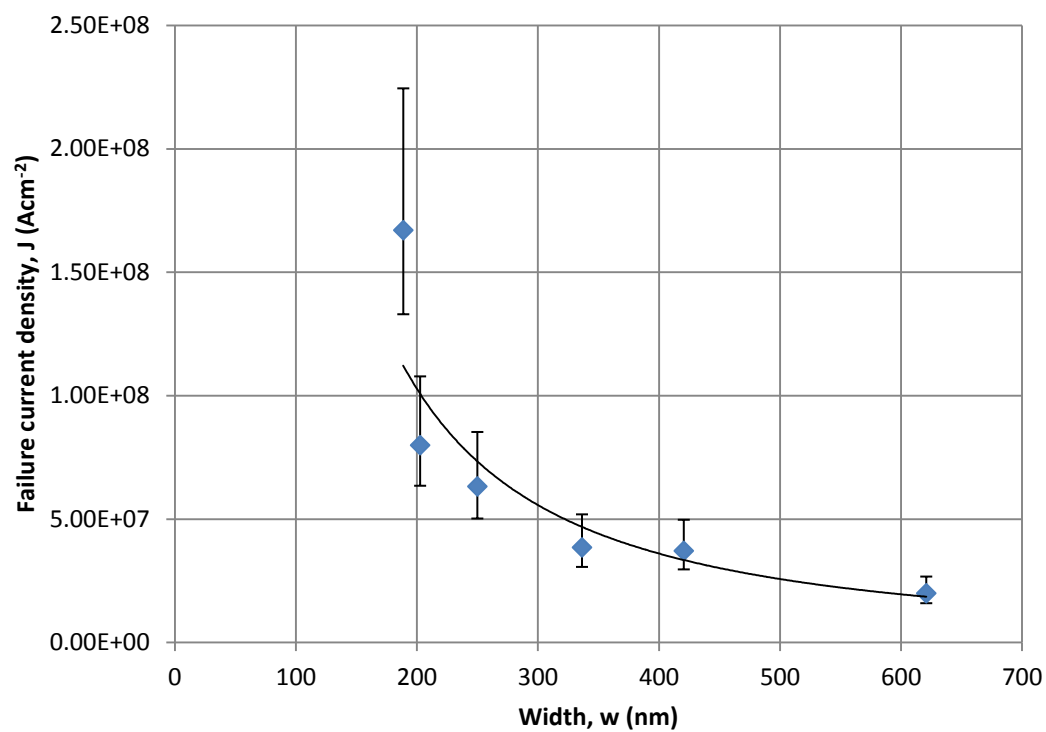


**Figure 21:** Electrical current stressing of a Cu-Si nanowire on Si(110). (a) Before failure. (b) After failure, i.e. a broken nanowire.



**Figure 22:** Analysis of failure current density trend with respect to the nanowire length. In this experiment, a single and long Cu-Si nanowire was used. Therefore, the experiment could be repeated several times while maintaining a consistent cross-section area of the nanowire.

The failure current density for different cross section areas of Cu-Si nanowires was also investigated. Six different Cu-Si nanowires self-assembled on the same Si(110) substrate were employed. The two nanoprobe that delivered the electrical current were spaced at  $\sim 20 \mu\text{m}$  from each other, and this spacing was maintained throughout the experiment by moving the substrate to position the nanowires under the probes vs moving the probes to new nanowires. Hence, it reduced the L uncertainty in the experiment. Nevertheless, the cross-section area of each nanowire was estimated using the method described in Appendix II. The results of the experiment are shown in Figure 23. The nanowire with the smallest area yielded an outlier point, which shows exceptionally high resilience to current stress. This outlier may be due to structurally different nanowire, e.g. a less defect and more crystalline nanowire would tolerate a higher current stress level. To overcome the irregularities of measurement, more data point will be needed. Nevertheless, the plot suggests a smaller width can carry a higher current density and such observations have been reported by other researchers, for example see Reference [80]. The authors explained that a smaller nanowire width conducts thermal heat to the Si substrate more efficiently than its larger counterpart. However, there will likely be a critical width where the nanowire below this value will fail at a lower current density [80]. Because of the limitation of nanoprobe, nanowires with  $< 100 \text{ nm}$  width cannot be measured with the system used in these experiments. Nevertheless, from the plot, we can see that the failure current density plateaus at  $2 \times 10^7 \text{ A.cm}^{-2}$ . The latter can be considered as the bulk failure current density value for  $\text{Cu}_3\text{Si}$ , which may have not been reported before.

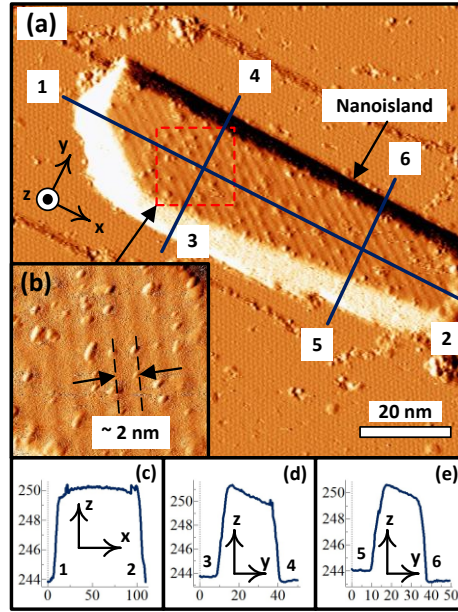


**Figure 23:** A plot of failure current density,  $J$ , against different nanowire widths. The bulk  $J$  value is estimated at  $\sim 2 \times 10^7 \text{ A.cm}^{-2}$ .

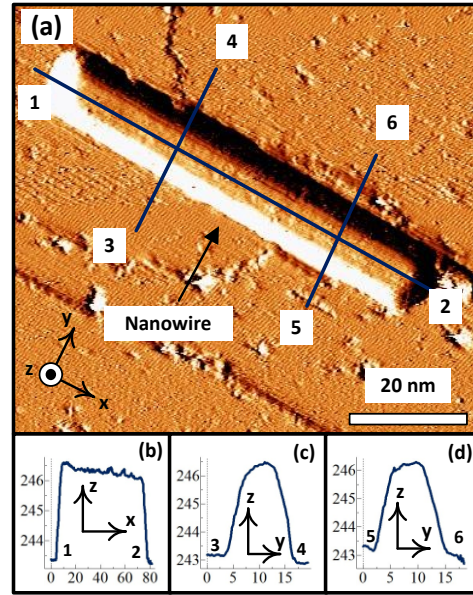
#### 4.3.4 Electrical Characterization of Sub 100 nm Cu-Si Nanostructures

For electrical characterization of sub 100 nm Cu-Si nanostructures, scanning tunneling spectroscopy (STS) measurements was employed. Two Cu-Si nanostructures grown on Si(110), as shown in Figures 24 and 25, were studied. The STM scans in the two figures are labeled to indicate their structural dimensions and surfaces. For simplicity and due to their shapes, the Cu-Si nanostructure in Figure 24 will be coined as a nanoisland while the nanostructure in Figure 25 will be coined as a nanowire.

The STS measurements were performed on three locations, which are represented as black dots in Figure 26a-b. A STS was performed each on the nanoisland, nanowire, and Si surface. The latter was used as a baseline to compare the  $\text{Cu}_3\text{Si}$  electronic properties. The three measurements can be identified by their different colors: Blue for the nanowire, Green for the nanoisland, and Red for the Si(110) surface. Each plot is an average curve obtained from twenty measured cycles obtained with a constant current bias of 100 pA and sample voltages swept from -1 V to 1V, as shown on the x-axis in Figure 26c. The y-axis in Figure 26c is the differential conductance,  $dI/dV$ , of the STS measurement which reflects a first order approximation of the local density of states (LDOS) [111]. Corresponding to these LDOS are the current-voltage (I-V) plots in Figure 27, which have the same color notations as in Figure 26. The STS measurements are briefly explained here. When the sample is positively biased, the occupied states of the tips tunneled into the unoccupied states of the sample and vice versa. Therefore STS is also a measurement of the number of states available in the conduction and valence bands.



**Figure 24:** (a) An STM image of a self assembled Cu<sub>3</sub>Si nanoisland on Si(110). The image was taken with tip biases of -2 V and 500 pA. (b) Inset shows a higher STM magnification on the area depicted by red dashed box. The scan area of the inset image was 20 nm × 20 nm and with the same tip biases as before. (c)-(e) Profile dimensions of the nanoisland that were obtained from the lines shown with numerical labels. The scales on the x-y-z axes are in nm, respectively.

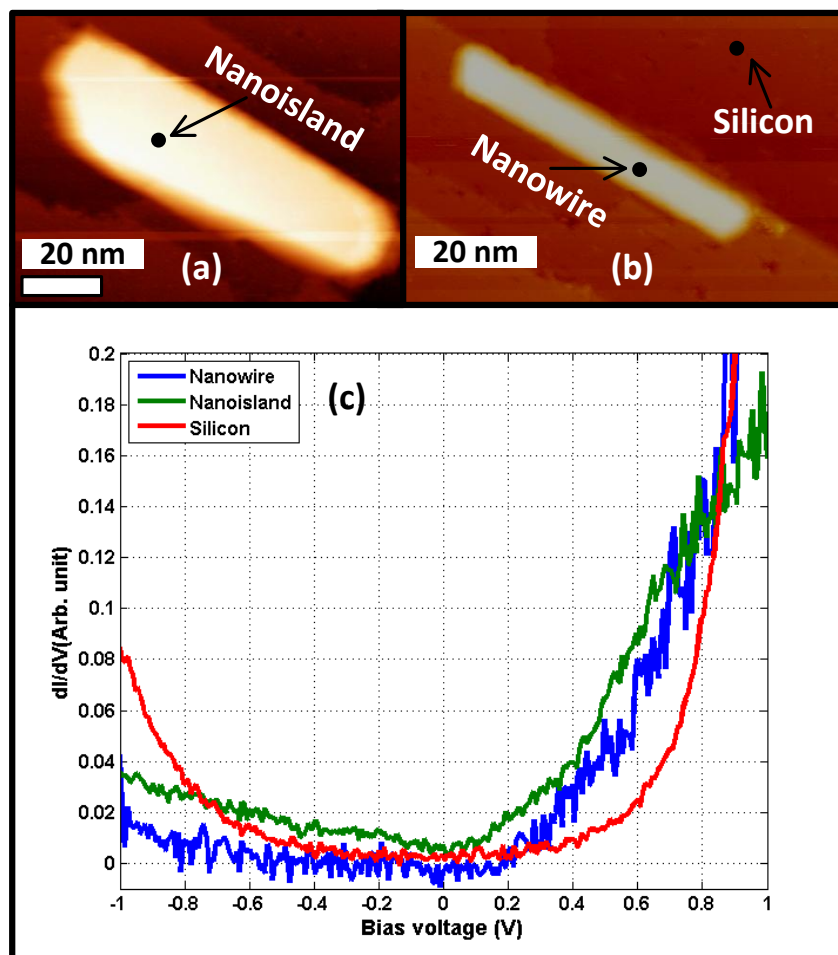


**Figure 25:** (a) An STM image of a self assembled  $\text{Cu}_3\text{Si}$  nanowire on Si(110). The image was taken with tip biases of -2 V and 500 pA. (b)-(d) Profile dimensions of the nanowire that were obtained from the lines shown with numerical labels. scales on the x-y-z axes are in nm, respectively.

LDOS of Si(110) in Figure 26c shows a semiconductor behavior with an electronic bandgap. An undoped, intrinsic, Si would have a LDOS symmetry along the Fermi level, which is at 0 V on the x-axis. However this was an n-doped Si(110) with more states in the conduction band that is to the right side of the Fermi level in the figure. The LDOS of Si(110) did not go to zero value on the y-axis and this was likely attributed to the non-ideal surfaces of Si(110), e.g. oxygen or water molecules adsorbates, that altered the Si surface states. Nevertheless we will use this Si(110) LDOS as a reference. Both LDOS of  $\text{Cu}_3\text{Si}$  nanowire and  $\text{Cu}_3\text{Si}$  nanowire in Figure 26c show more available states in the conduction band. As mentioned before,  $\text{Cu}_3\text{Si}$  was found to be metallic on larger structures and therefore more electronic

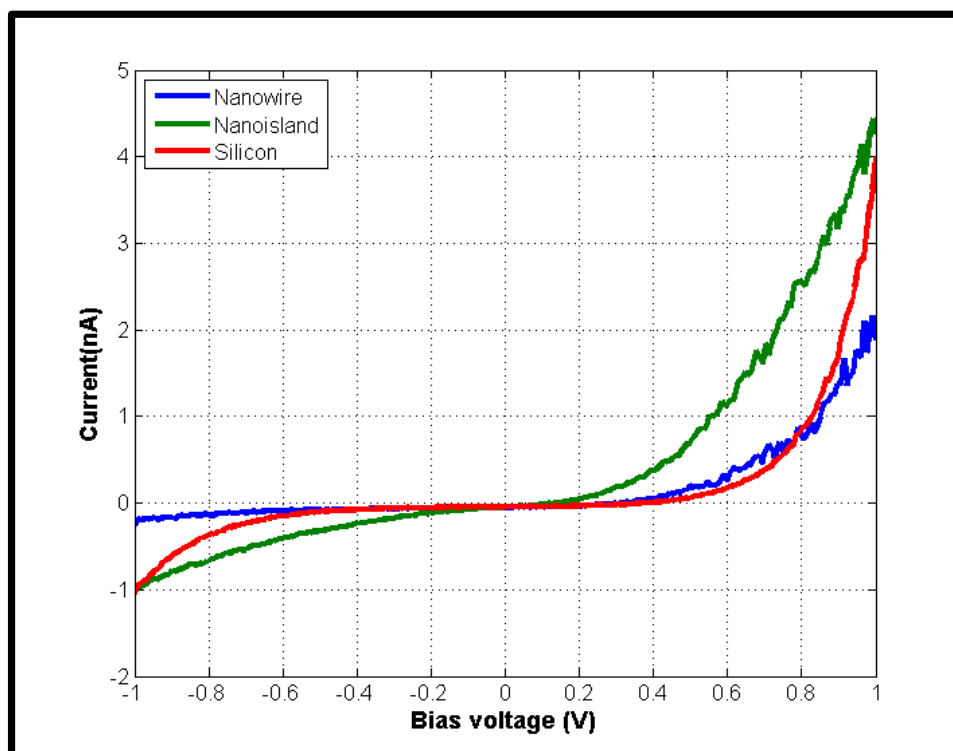
states in the conduction band in Figure 26c are reasonable. The electronic states in the valence band for both structures were found to be lower than the Si(110), which are seen in the figure. Although the LDOS for the two nanostructures appeared to be similar, they are actually different. First, LDOS for the nanoisland did not approach zero value, albeit very near to zero. Such characteristic shows a semi-metal behavior, which might be easier to distinguish from the I-V plot in Figure 27. Since the semi-metal state is not known to exist on larger  $\text{Cu}_3\text{Si}$  structures, the effect may be due to quantum confinement in z-direction, since the dimension along this direction was the smallest,  $\sim 10$  nm. This semi-metal observation also suggests that the  $\text{Cu}_3\text{Si}$  nanoisland could potentially transform from a semi-metal to semiconductor. In fact, this speculation is supported by the STS measurements of the nanowire in Figure 25, as shown in Figure 27c. The LDOS approached a zero value and appeared to have a bandgap structure. It may be easier to distinguish between semi-metal and semiconductor behavior from the I-V plots in Figure 27. As compared to the Si curve, which shows characteristics of semiconductor behavior, the I-V curve for the nanowire appeared similar, especially in the conduction band region. However, in the valence band region, the I-V measurement was more resistive than the Si substrate. For the nanoisland, the I-V data did not show metallic or semiconductor characteristics, instead it was in between the both, which is semi-metallic.

The results indicate possible quantum confinement due to size effects on  $\text{Cu}_3\text{Si}$  nanostructures on Si(110). However all STM images presented in this paper were made with -2 V sample bias. Due to technical difficulties, the positive sample biased images were not obtained. Future work is needed to investigate these nanostructures at positive biased and compare the results with the negative biased images.



**Figure 26:** Location of the STS measurements on (a) the nanoisland of Figure 2 and (b) on the nanowire and Si surface of Figure 3. (c) STS plots with 100 pA constant current biased.





**Figure 27:** STS I-V plots corresponding to Figure 26c. The red curve shows a semiconducting behavior of Si surface. The blue curve also shows a semiconducting behavior whereas for the green curve shows a semi-metallic behavior.

#### 4.4 Summary

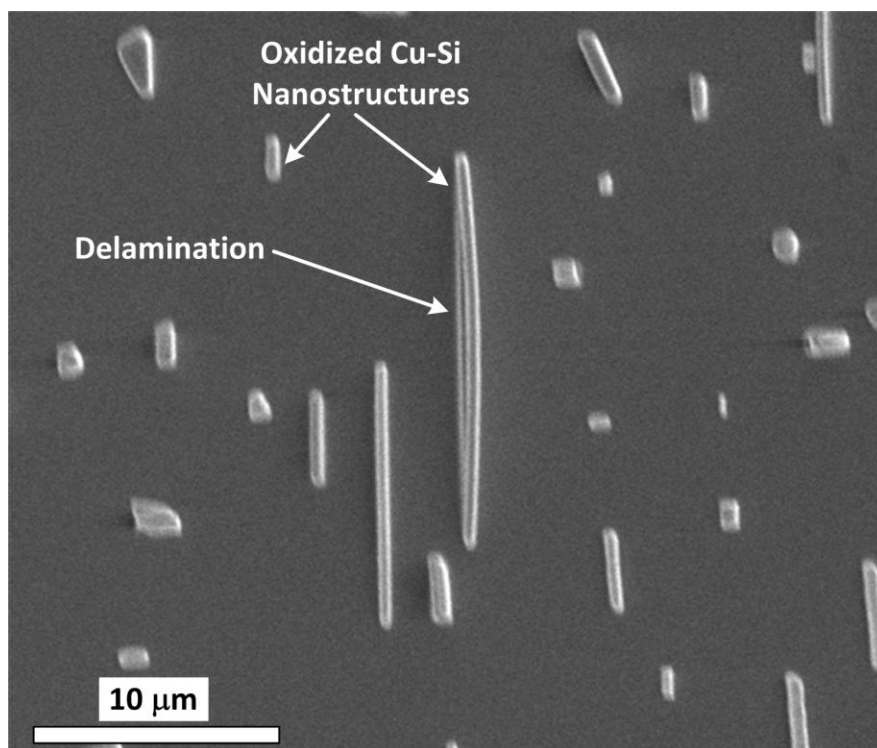
The third objective of this thesis was to perform electrical characterization on Cu-Si nanostructures. The nanowire resistivity for Cu<sub>3</sub>Si is  $\sim 30\text{-}50 \mu\Omega\cdot\text{cm}$ . The characterization has also revealed several interesting properties. From Figure 22, the maximum failure current density was estimated at  $> 1 \times 10^8 \text{ A}\cdot\text{cm}^{-2}$ , which is comparable to the current density for single crystalline NiSi nanowires [112]. The study also suggested (via estimation in Appendix II) that the bulk value for failure current density of Cu<sub>3</sub>Si is  $\sim 2 \times 10^7 \text{ A}\cdot\text{cm}^{-2}$ , which has not been reported before. We have also observed changes in the LDOS for Cu<sub>3</sub>Si nanostructure from semi-metallic to semiconducting when the Cu-Si nanostructure have sub 10 nm dimensions (in this case the height).

## 5. MATERIAL STUDIES OF OXIDATION OF SELF ASSEMBLED CU-SI NANOSTRUCTURES ON SILICON (001)

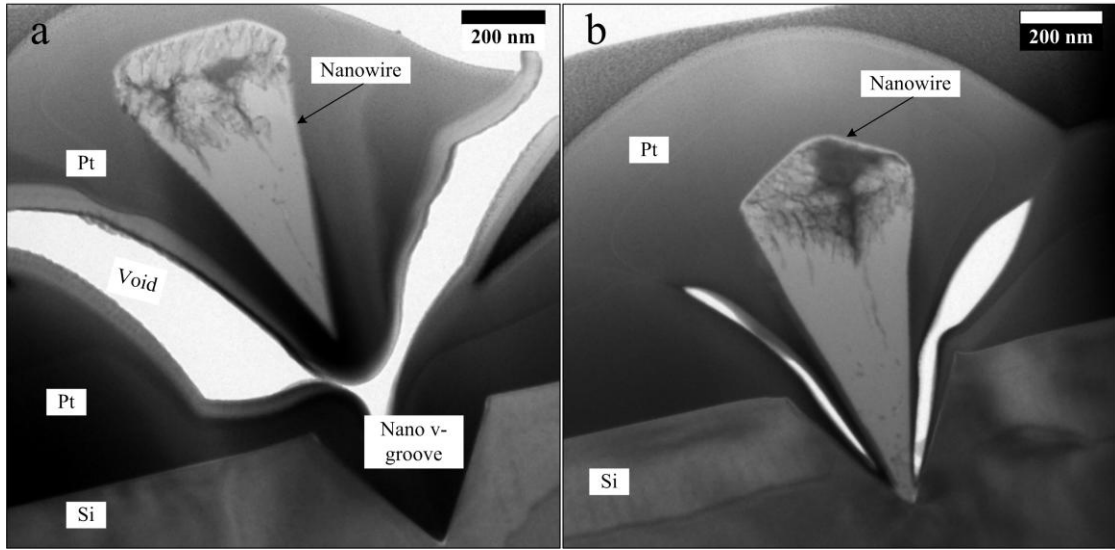
### 5.1 Introduction

One of the discoveries made during this PhD work was how rapid the self assembled Cu-Si nanostructures oxidized in ambient condition. A discarded sample of Cu-Si nanostructures left at room temperature and ambient conditions for three weeks was later found to have significant changes on the surface (see Figure 28). As compared to typical Cu-Si nanostructures as seen in Chapter 2, these nanostructures like those in Figure 28 appeared to have grown in volume until one of the nanowires in the figure appeared to be delaminated from the substrate. The storage under ambient conditions was speculated to lead to oxidation process that strongly modifies the sample's morphology.

Two 'oxidized' Cu-Si nanowires were preliminary analyzed with TEM to verify their chemical composition, which are shown in Figure 29. Using XEDS analysis (not shown here), the majority of  $\text{Cu}_3\text{Si}$  material was found on the top portion of the nanowire while the majority of oxide material was found to be at the lower portion of the nanowire. Therefore, the XEDS data corroborated our speculation that the Cu-Si nanostructures were oxidized. However, instead of  $\text{SiO}_2$ , the XEDS data indicate that the bottom part of the needle-like structure consists of a mixture of  $\text{SiO}$  and  $\text{SiO}_2$ .



**Figure 28:** A SEM micrograph of self assembled Cu-Si nanostructures after left in ambient condition for three weeks.



**Figure 29:** Cross sectional TEM images of two oxidized Cu-Si nanowires with (a) a nanowire that is still attached to the Si substrate and (b) another nanowire that is completely delaminated from the Si substrate.

Although studies on thin film metal silicide oxidation are common such as in References. [71, 73, 113], there is a lack of published chemical data on oxidation of Cu-Si nanowires on Si(001). While oxidation of thin film  $\text{Cu}_3\text{Si}$  has been studied in details by Cros *et al.*, in Reference [87] and Harper *et al.* in Reference [73], the thin film results are not consistent with our TEM data. In particular, the oxidization of self assembled Cu-Si nanowires on Si(100) at room temperature can result in v-grooves with sidewalls formed by  $\text{Si}\{111\}$  planes, which has not been reported elsewhere. The Cu-Si nanowire oxidation on Si(001) gives the same effect as anisotropic wet etching without involving wet chemicals. Thus, this process is referred as solid anisotropic etching. However, there is still a lack of fundamental understanding of the Cu-Si nanowires and Si interaction during the oxidation process, which results in v-shape grooves that may be of technological interest in nanofabrication. Thus, new experiments were

conducted to investigate the basic chemistry anisotropic properties of the solid etching of self assembled Cu-Si nanowires on Si(001), which are the focused of this chapter.

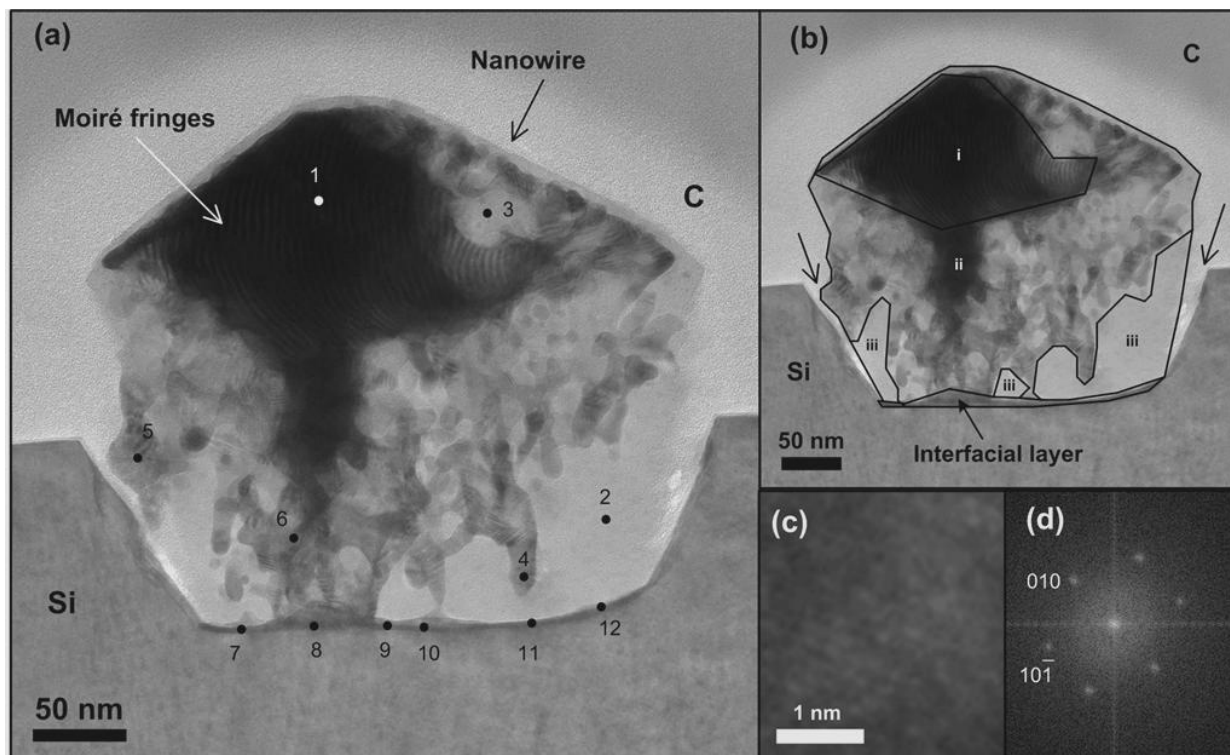
## 5.2 Experimental Procedures

The procedure to prepare self assembled Cu<sub>3</sub>Si nanowires on Si(001) is the same as in Chapter 2. After fabricating Cu-Si nanowires on Si(001), the sample was removed from the vacuum chamber and left to oxidize at 22 °C with a humidity of 43 % in a laboratory environment. An oxidized sample was analyzed after 1, 3 and 7 weeks of oxidation. For each analysis, a Transmission Electron Microscope (TEM) sample was prepared with a focused Ga ion beam (FIB) by first applying a carbon (C) coating as a protective layer and then ion milling to obtain a thin cross-sectional sample of the nanowires. FIB preparation was performed with a Zeiss 1540XB FIB-SEM at the Electron Microscopy Center (EMC) at Argonne National Laboratory. All three specimens were studied with TEM using a Tecnai F20ST AEM at the EMC. X-ray energy dispersive spectroscopy (XEDS) was also conducted with the TEM.

## 5.3 Results and Discussion

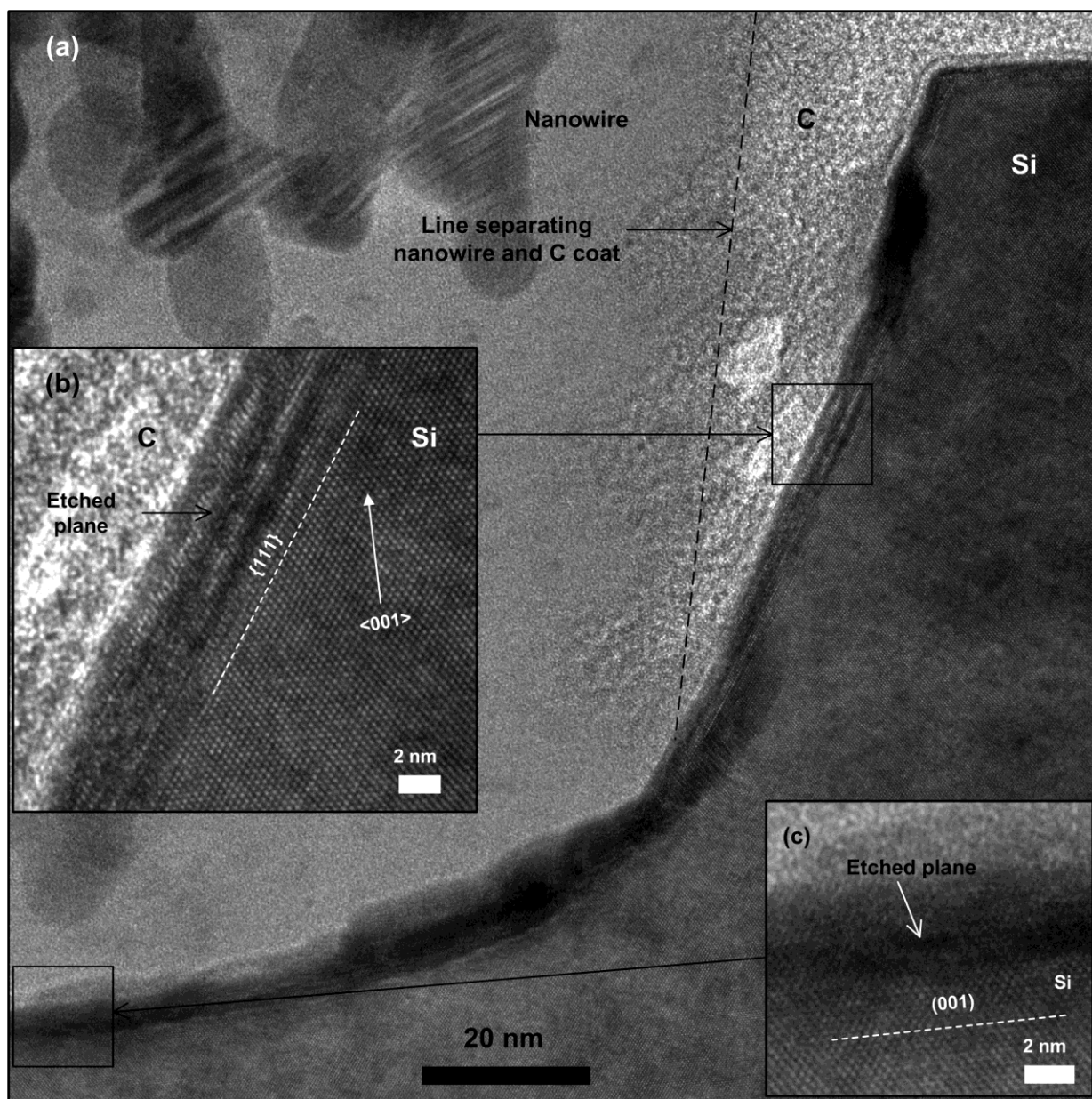
After oxidizing for one week, a random self assembled Cu-Si nanowire was analyzed. Figure 30a shows a cross sectional TEM image of the nanowire, labeled as Sample A. XEDS analysis (via Emispec ESVision standardless analysis) was performed at several locations of the surface, as indicated by numeric labels in Figure 30a, and the results are shown in Table III. Based on the XEDS analysis, we may divide the nanowire into three different regions, labeled as 'i', 'ii', and 'iii' in Figure 30b. Region 'i' was mostly dark in contrast and possessed Moiré fringes. These fringes were observed for the pristine Cu-Si nanowire shown in Figure 1. Therefore region 'i' may be the remnant of an original single crystalline Cu-Si nanowire. This observation is consistent with the XEDS data on location number 1 from Table III,

which suggests an  $\eta$ -Cu<sub>3</sub>Si (eta) phase with some oxygen. In region 'ii', several XEDS data points show various combinations of Cu, Si, and O ratio. Lattice fringes were observed in several nanocrystalline areas of region 'ii', such as in Figure 30c. The XEDS data for position 5 (Figure 30a) and the lattice images (see Figures 30c and 30d) in that area are consistent with interpreting that area as  $\kappa$ -Cu<sub>7</sub>Si (kappa) surrounded by SiO<sub>2</sub>. It should be pointed out that the lattice images throughout region 'ii' are consistent with  $\kappa$ -Cu<sub>7</sub>Si (kappa) phase. Nevertheless, we are uncertain whether the nanowire started as a monolithic material (i.e. single phase) that gradually transformed into kappa phase during the oxidation. According to the reactions in equations (1) and (2), Si would have formed SiO<sub>2</sub> during the oxidation, which could result in region 'iii'. XEDS data on this region 'iii' and the images are consistent with an amorphous SiO<sub>2</sub> phase. The most plausible source of the nanocrystallites in region 'ii' is the Cu-Si nanowire. The actual mechanism on how pieces of single crystalline Cu-Si dislodged from the nanowire (region 'i') and into region 'ii' is unknown and may be of interest in future studies. An attempt was made to perform XEDS analysis on the interfacial layer (locations 7 – 12) as shown in Figure 30a. All the data on the interface show SiO<sub>2</sub> layer. It was expected that the interfacial layer contained Cu from the reactions described by equations (1) and (2). We also cannot discount the possibility that the XEDS beam spot might have drifted upwards into region 'iii' during the testing since the interfacial layer was very thin and had similar width to the XEDS beam diameter. Oxidation at the interfacial layer will result in an accumulation of SiO<sub>2</sub> in region 'iii' (see Figure 30b). As can also be clearly seen, the nanowire grew in volume and height. Simultaneously, the reaction also penetrates into the Si substrate, which results in the solid etching after the nanowire is released from the substrate. HRTEM images in Figure 31 show that etched boundaries for Sample A are (001) and {111} boundaries. Furthermore, the black dashed line indicates where the nanowire delaminated from the Si substrate. These HRTEM results verify that the oxidation of Si via Cu-Si indeed behaves similar to anisotropic etching.



**Figure 30:** Cross section TEM micrograph of a self assembled Cu-Si nanowire on Si(001). (a) XEDS positions for Sample A obtained during week one of oxidation. Corresponding XEDS data are given in Table III. (b) Outlines in solid black to show different regions of the nanowire in (a) based on their materials composition. Region 'i' consisted Cu<sub>3</sub>Si with some O, region 'ii' consisted a mixture of Cu-Si and O, and region 'iii' consisted mostly Si-O. (c) A HRTEM view around XEDS position 5 shows a nanocrystallite. Several nanocrystallites can be found throughout region 'ii'. (d) A fast fourier transform (FFT) of a nanocrystallite found in region 'ii' shows a  $\kappa$ -Cu<sub>5</sub>Si phase with its crystallographic direction along [101].

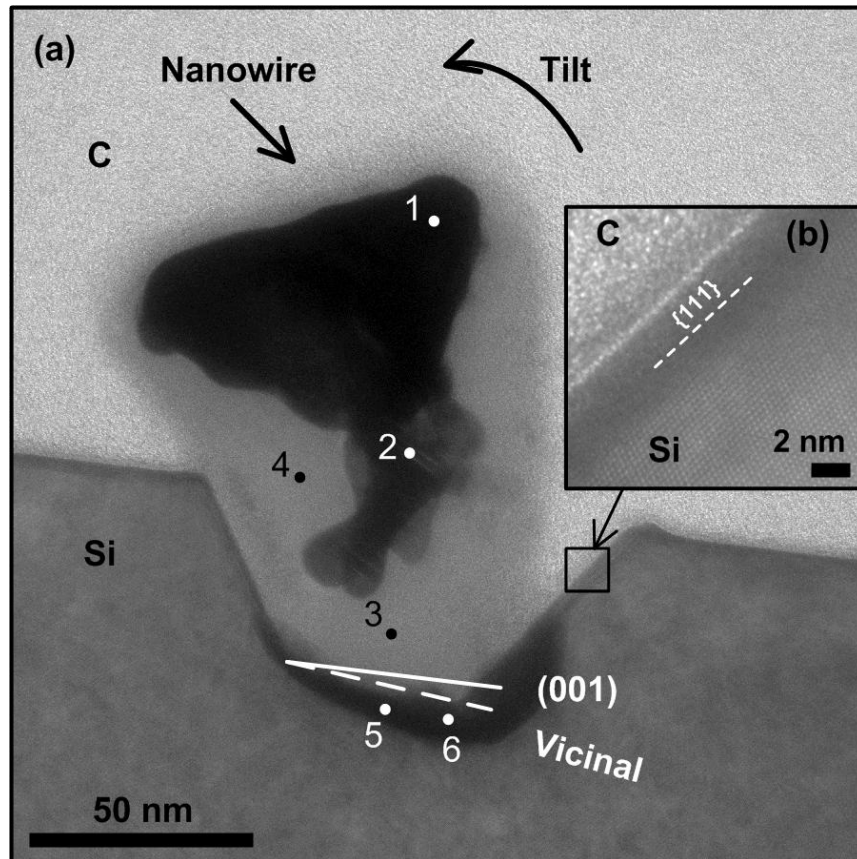




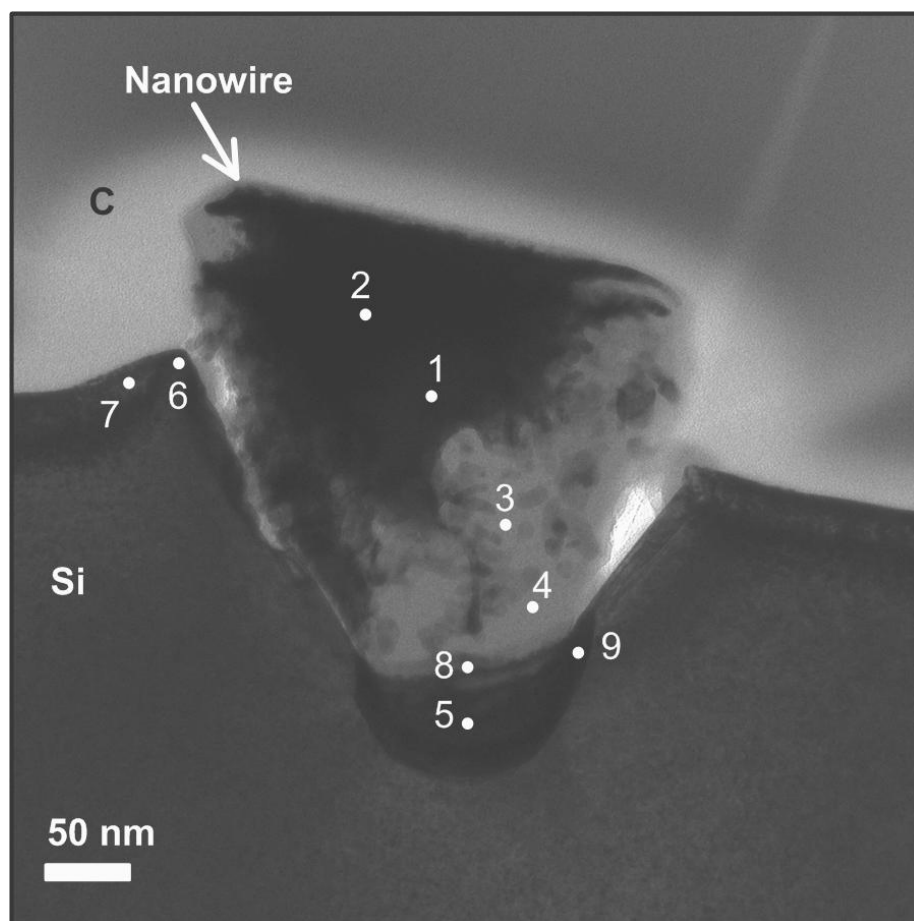
**Figure 31:** (a) A high resolution TEM (HRTEM) view on the lower right hand side of Sample A. (b) The Si edge along {111} shows an anisotropic etching effect. (c) The lower boundary of Sample A shows Si(001).

After two weeks of oxidation, another nanowire, labeled Sample B, was analyzed with TEM as shown in Figure 32. Similar to Sample A, the nanowire was on the Si substrate and coated with C, which served as a protective layer from ion milling damage. Again, XEDS analysis was performed on several spots denoted by numeric labels in the figure and the results are given in Table III. At XEDS number 1, neglecting the 15 atomic % O, the Cu to Si ratio was roughly 3.7 to 1. Accounting for XEDS sampling error, the region may be a mixture of O and Cu-Si material. At XEDS number 2, towards the center part of the nanowire, a higher O content about 44% was detected, which is expected since the area was closer to the oxide layer. Because of the mixture of O and Cu-Si materials in locations 1 and 2, the two regions are similar to regions 'i' and 'ii' in Sample A. XEDS data on locations 3 and 4 show an oxide region with what appeared to be a SiO phase, albeit with a minor Cu concentration. The oxide phase detected here was different than that found in Sample A, which had a SiO<sub>2</sub> phase. It may appear that the oxide phases evolved from SiO<sub>2</sub> to SiO. However to resolve this evolution of oxide phases, another analytical tool is required such as 2p core level X-ray photoemission spectroscopy (XPS) system.[114] HRTEM analysis shows that the oxidation etches along the Si{111} boundaries, as shown in inset (b) of the figure. From the TEM micrograph, it can be seen that the nanowire is tilted to the left side as labeled by an arrow. The reason for this tilt is that the Si(001) substrate had a 4° vicinal miscut. Referring to the micrograph, the (001) plane is represented by a white line whereas the vicinal miscut is shown as a white dashed line. It may be noted that latter was the actual (001) surface. Therefore the TEM micrograph suggests that the nanowire also oxidized along the Si(001) plane in addition to the Si{111} planes. The etch plane is significant to the release of the nanowire from the substrate since etching along the {111} direction will result in delamination for Si(001). Because of the miscut, the nanowire had more Si material to oxidize as the nanowire-Si interface moved from left to right. As a result, the nanowire grew taller on the right side and resulted in the tilt.

After oxidizing for seven weeks, a nanowire (Sample C) was analyzed with TEM as shown in Figure 33. From the figure, the etched Si formed anisotropic planes along (001) and {111} boundaries. On the left side of the image, the substrate surface curves upwards; this was likely formed during Cu deposition on Si. This effect also can be seen in figure 1b as Si wets on the edge of the nanowire. XEDS data for this sample is given in Table III. In this sample, a TEM grid of Cu material was used. Therefore the XEDS data in the table have been processed to remove background noise due to the Cu TEM grid. XEDS locations number 1 and 2 comprised various contents of Cu, Si, O, which was similar to region ‘ii’ in Sample A. On locations 3 and 4, the Cu content was negligible with prominent Si-O presence. At location number 8, the nanowire-Si interface, a high Cu atomic weight was detected. This suggests that Cu was present during the Si oxidation process (see equations 1 and 2). Surprisingly after seven weeks of oxidation, the sample did not produce a complete v-channel as seen in Figure 29. A possible reason is that the temperature and humidity in the prior experiment were unregulated at atmospheric conditions during a warm and humid period of the year. Therefore these factors may have resulted in a higher rate of oxidation, and thus promoted the release of the nanowire from the substrate.



**Figure 32:** (a) A cross section TEM micrograph of a self assembled nanowire (Sample B) obtained at week two of oxidation. Numerical positions show the location of XEDS data, which are given in Table III. (b) A HRTEM view that shows the etched Si plane is along  $\{111\}$ , which is anisotropic.



**Figure 33:** A cross section TEM micrograph of a self assembled nanowire (Sample C) obtained at week seven of oxidation. The numeric labels indicate XEDS positions and the data are given in Table III.

**Table III:** XEDS data obtained during week one, three and seven of oxidization of self assembled Cu-Si nanowires on Si(001)

	Position	Cu at%	Si at%	O at%
Sample A	1	73	21	6
	2	0	38	62
	3	16	36	48
	4	13	32	55
	5	53	23	24
	6	37	23	40
	7	6	37	57
	8	13	35	52
	9	4	36	60
	10	17	32	51
	11	4	36	60
	12	0	34	66
Sample B	1	79	21	0
	2	59	25	16
	3	18	38	44
	4	2	38	60
	5	15	40	45
	6	7	40	53
	7	9	87	4
	8	5	90	5
Sample C	1	47	25	2
	2	79	21	0
	3	0	44	56
	4	0	45	55
	5	14	84	3
	6	10	53	37
	7	0	100	0
	8	15	48	37
	9	0	98	2

## 5.4 Summary

Oxidation of self-assembled copper silicide nanowires on Si(001) were studied in detail with HRTEM and XEDS techniques. As expected,  $\eta$ -Cu<sub>3</sub>Si phase was detected in sample A due to its widely reported phase from other similar experiments. However, a  $\kappa$  phase was also detected in Sample A, which is a new observation. Therefore the oxidation process of the nanowire involving its Cu<sub>3</sub>Si, Si, and O may be slightly different than those described by Harper *et al.* in Reference [73]. Furthermore, SiO was detected in more aged specimens (Samples B and C) instead of the SiO<sub>2</sub>, which is predicted in the aforementioned predicted reactions and also seen in Sample A. The incomplete oxidation state of SiO may be due to the scarcity of Cu-Si materials at the Si boundary in the older specimens. It may be noted that Cu-Si, Si and O must be present for the oxidation process to occur. Therefore, the separation between Cu-Si and Si due to an accumulating Si-O layer will reduce the chances of oxidation. Since the oxidation will only occur where Cu-Si and Si are in physical contact (in addition to oxygen), the Cu-Si nanowires behaved like a negative template to oxidize the Si material. The resultant oxidized Si substrate forms boundaries along Si{111}, which resembles an anisotropic etching. The Si{111} planes also appeared relatively straight. However, future analysis will be needed to characterize the surface roughness. Given sufficient time and thermal energy, the oxidation will eventually form a 'v' groove without wet etchants. Hence, oxidation of Cu-Si nanowires on Si is a solid-solid reaction. Thus, we named the process as solid anisotropic etching, and can potentially be an alternative form of Si anisotropic etching in the future.

## 6. ATOMIC SCALE STUDIES OF SILICON (110) SURFACE RECONSTRUCTION

### DUE TO COPPER

#### 6.1 Introduction

Although the primary focus of this thesis was to study self assembled Cu-Si nanostructures on Si with e-beam evaporation method, the changes to Si surfaces due to the Cu deposition were quite significant. These changes occurred at atomic scale, whereby the surface reconstruction of a clean Si(110) transformed into a long range order  $2.3 \times 2.3$  superstructure surface reconstruction with chiral-like morphology. A clean and thermally treated Si(110) surface at  $> 550^\circ\text{C}$  will form a  $16 \times 2$  structure [115, 116]. Another surface structure that is also commonly observed at the same annealing temperature on a clean Si(110) is  $(17,15,1) 2 \times 1$  structures [116, 117], which has the same structural units to the  $16 \times 2$  structure [117]. The former comprises staircase terraces while the latter comprises up-down terraces, and both have the same structure and periodicity [117]. Yamada, *et al.* in Reference [118] determined that Si(110)  $16 \times 2$  arrays were made of Si atoms which existed in ‘pair of pentagons’ or PPs. Unorganized PPs are also common on clean Si(110) [116]. Research on contamination of Si(110) surfaces with nickel (Ni) indicates multiple surface reconstructions, e.g.  $5 \times 4$  [81, 82],  $1 \times 2$  [81, 83] and  $1 \times 5$  [81, 83]. Other metals influencing the surface reconstruction of Si(110) have also been reported, e.g.  $4 \times 1$  due to Silver (Ag) [84], and  $4 \times 5$  and  $2 \times 5$  due to Copper (Cu) [85].

While studies on Si surface reconstructions due to Cu were extensively explored for Si(111) [106, 119-122], only a few works were published for Si(110), see for example van Loenen *et al.* in Reference [85] and Ikeda *et al.* in Reference [123]. The former reported a Cu induced Si(110)  $5 \times 1$  surface reconstruction. However, there was a lack of STM images to show the reconstruction. On the other hand, the work by Ikeda, *et al.* focused on the growth mechanics of Cu structures on the Si(110) and not on the



Si surface reconstruction. Therefore, this chapter will investigate in more atomistic detail Cu influenced Si(110) surface reconstruction.

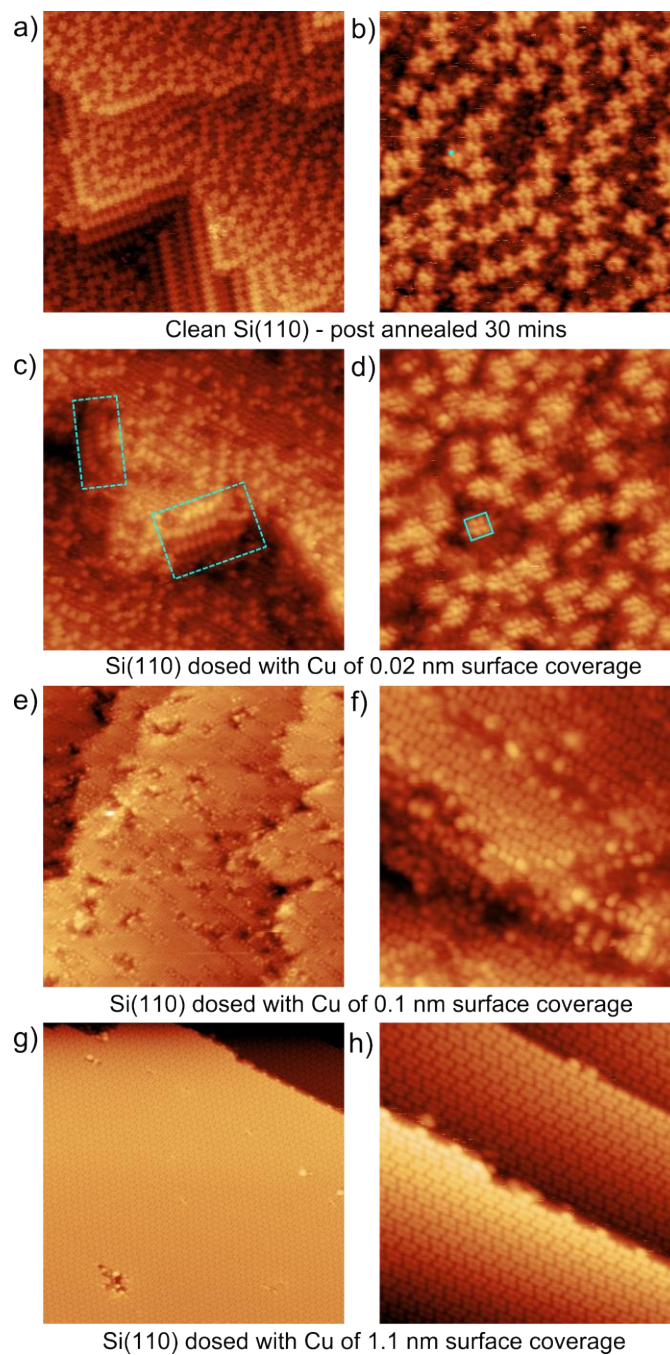
## **6.2 Experimental Procedures**

All experiments described in this paper were conducted on a  $10 \times 3$  mm precut sample from a 3 inch n-type doped Si(110) wafer having 1-10  $\Omega\cdot\text{cm}$  resistivity. Each precut Si sample was rinsed with isopropyl alcohol (IPA) and dried with nitrogen gas before mounting into a Molybdenum holder and loading into an ultra high vacuum (UHV) system. In the UHV, each sample was degassed at 600°C for > 12 hours to remove surface hydrocarbons. Then, the sample was flash heated at  $\sim 1200$  °C for 30 seconds and repeated to a total of three times to strip the native oxide from the surface. Cu was then evaporated from a clean Molybdenum (Mo) crucible onto the substrate. It should be noted that to the best of our efforts, the Si(110) was carefully prepared to avoid or minimize contaminations that might affect the surface reconstruction study. However, we cannot rule out the possibility that a small amount of contamination might have occurred. To verify whether a contamination, an AUGER analysis would be needed but was not performed in this study as the STM did not have such capability. Scanning tunneling microscopy (STM) was used to analyze the surface of Si(110) before and after Cu deposition with an Omicron Veeco multiprobe system located in the Center for Nanoscale Materials (CNM) at the Argonne National Laboratory (ANL), IL, USA, see Chapter 4.2.3 for more details.

### 6.3 Results and Discussion

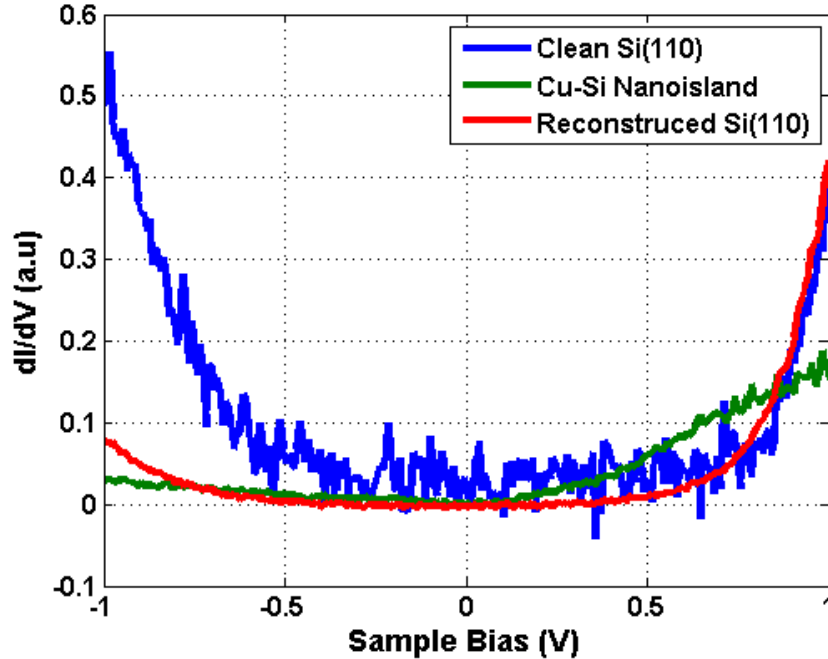
A clean Si(110) surface usually possessed domains with  $16\times 2$ ,  $(17,15,1) 2\times 1$  and PPs, as shown in Figure 34a and b, respectively. After depositing Cu of 0.02 nm surface coverage on the Si, the aforementioned three domains began transforming, as shown in Figure 34c. Clearly visible on the surface is newly observed streaks of parallel arrays, which highly suggest that the Si surface has reacted with Cu. The ‘stair-case’  $(17,15,1) 2\times 1$  domain in Figure 34c appeared to be on the onset of disintegrating. Also, angular features of Si step edges seen on a clean sample are no longer prominent after the first Cu dose. A higher resolution image in Figure 34d shows clusters of four atoms (in a blue square) that did not appear to be that of PPs but appeared to be consisting of four atoms. Unlike PPs, these new group of four atoms may exist alone. Therefore, during the Cu deposition, PPs were likely to undergo transformation into individual groups of four atoms. A further dose of 0.1 nm Cu surface coverage (5 minutes) and a further post annealing of 20 minutes resulted in a different surface reconstruction as shown in Figure 34e-f. The surface appears to be a stack of ‘plates’ with rough step edges. Figure 34f shows a clearer picture of these new features, which shows more prominent clusters of four atoms that are aligned in a periodic manner. At this stage, the surface reconstruction was still incomplete and plagued with hole defects. It is uncertain whether the bright features in the figure were that of unreacted Cu or Si atoms. A final reconstructed surface is obtained by dosing the surface with Cu of 1.1 nm surface coverage while annealing the substrate for 20 minutes. This experiment was performed separately on a clean Si(110) sample as we discovered that a continuous Cu dosing on the sample would produce a uniform surface as shown in Figure 34g-h. From the figures, all atoms appeared to have reacted and formed periodic structures with parallel step edges. Figure 34g shows groups of four atoms in tightly packed periodic formations on this newly reconstructed surface. The size of the new domain is very large and covers the micrograph viewing area, which implies a long-range ordered surface reconstruction. The electronic states of the reconstructed

surface is compared to a clean Si(110) surface and a Cu-Si nanoisland, as shown in Figure 35. As can be seen, after Cu deposition, the density of states (DOS) in the valence band of the Si(110) were reduced to a level comparable to that of a copper-silicide nanoisland. Nevertheless, studies of the electronic structures of the Si(110) surface before, during, and after Cu induced surface reconstruction were not extensively performed and are not discussed in this thesis as it was outside the scope of the research. The purpose of the  $di/dv$  plots was to compare. Furthermore, the atomic elements of the reconstructed Si(110) surface have not been identified. Therefore, electronic structure and atomic elements of the reconstructed surface this will be subjects of future investigations.



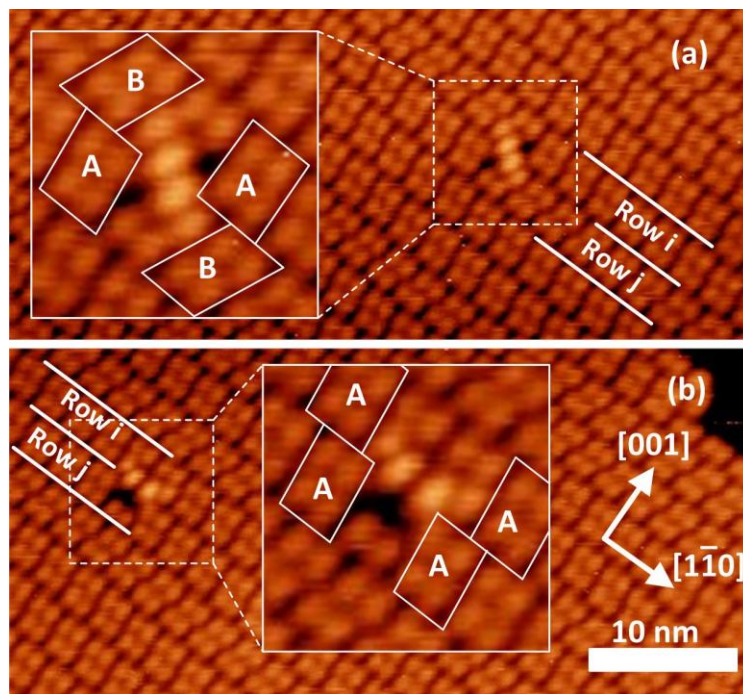
**Figure 34:** (a)-(h) STM micrographs showing a morphology of a clean Si(110) to a  $2.3 \times 2.3$  superstructure by gradual dosing of Cu. (a)-(c) Surfaces of a clean Si(110). (a) Rectangular boxes denote  $16 \times 2$  and  $(17,15,1)2 \times 1$  surface reconstructions. (b) An enlarged scan of an interface between the

aforementioned two domains in (a). (c) A micrograph of pairs of pentagon (PP). (d)-(f) Surfaces of a Si(110) after dosed with a 0.016 nm surface coverage of Cu. (d) (17,15,1)2×1 reconstruction began to disintegrate and periodic arrangement along <110> began to take place. (e) PPs are no longer observed. (f) An enlarged micrograph of (e) showing cells of four atoms. (g)-(h) Surfaces of Si(110) after dosing with 0.1 nm surface coverage of Cu. (g) Periodical arrays of atoms along <110> are more prominent. (h) An enlarged scan showing details of the surface, which is a pre-formation of a  $2.3 \times 2.3$  superstructure. (a)-(b) STM biased at 1.5V and 250 pA, (c) at -2 V 100 pA, (d) at 2 V and 100 pA, (e) at 1.2 V and 100 pA and (f) at 1 V and 100 pA.



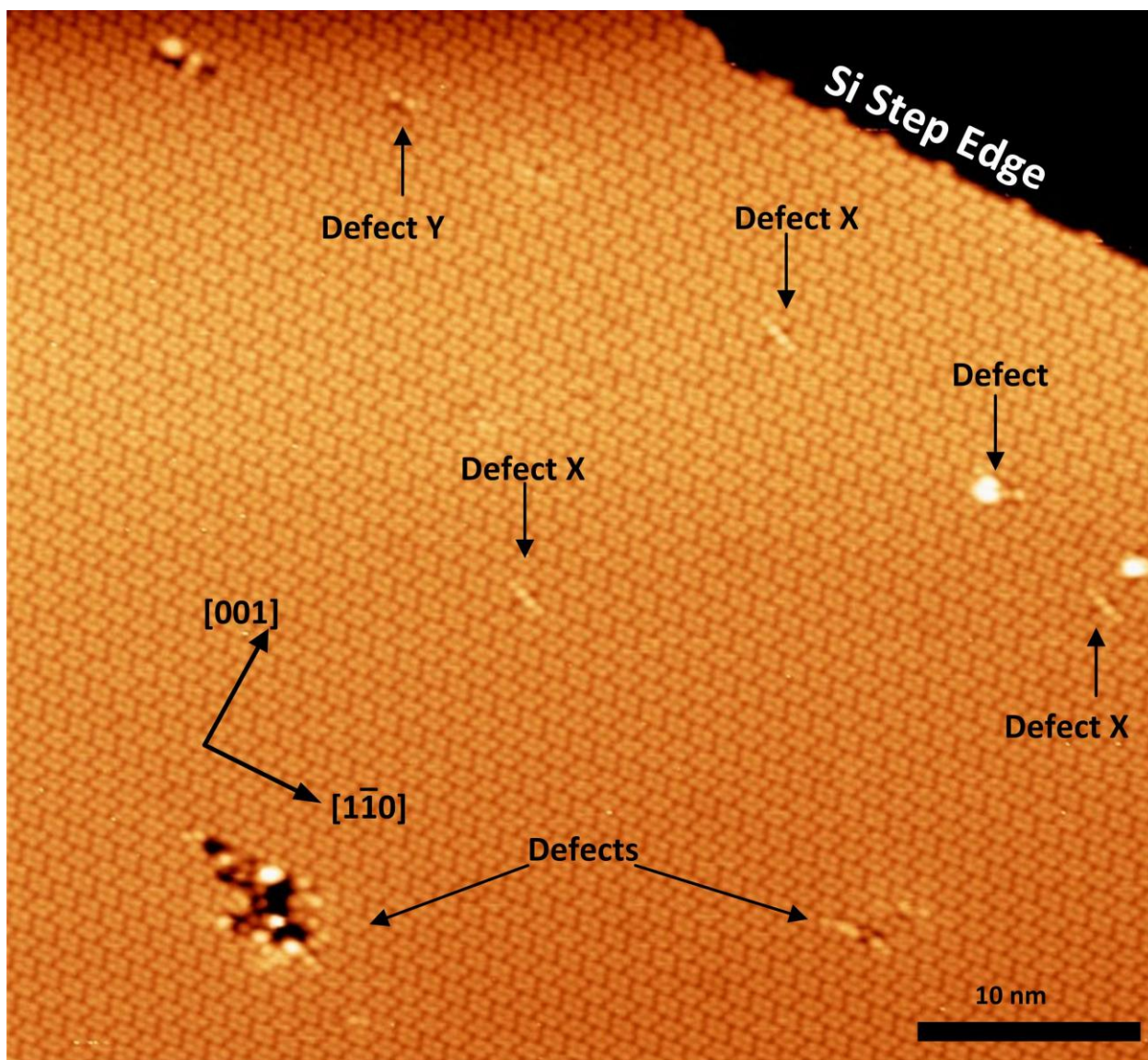
**Figure 35:** Differential conductance (dI/dV) plots for a clean Si(110), reconstructed Si(110), and a Cu-Si nanoisland.

The final reconstructed Si(110) surface had unit cells with different oriented rhomboids, which are shown as type A and B in Figure 36. The unit cells forms homogenous row of (AAA...) or (BBB...) along  $\langle 1\bar{1}0 \rangle$  direction as seen in Figure 37. Each row was of either rhomboids type A or B. However surface defects could modify the stacking order in the aforementioned direction. Presently, little is known about the origin and atomic material of these surface defects. Referring to Figure 36a, stacking orders along the two rows were interrupted by a surface defect, causing (BBB...) stacking to change to (AAA...) stacking in row i and vice versa in row j. This surface defect, denoted as type X, has two radial structures that appear to be connecting the two consecutive rows. Another type of surface defect, which is seen in Figure 36b and denoted as type Y, seems to have similar radial structure as type X. The two radial structures in type Y defect appear to connect to the same row instead of crossing over to another row like type X. Nevertheless, this type Y defect does not change the stacking order along the row direction. To gain insight into these stacking orders and defects, we inspected a larger surface area. The distribution of rhomboid A and B cells was counted in Figure 37 and found to have 21 counts and 22 counts, respectively. We excluded the rows with defects that caused (...AAABBB...) and (...BBBAAA...) stacking orders in the  $[1\bar{1}0]$  direction since the two rows constituted both types of cell. Although a larger sampling size is preferred, our preliminary study suggests the distribution of type A and B cells was almost equal. This indicates that the surface reconstruction had no preference towards either A or B orientations.



**Figure 36:** (a) STM micrograph of a surface defect, which is denoted as type X, that causes row stacking order in  $[1\bar{1}0]$  direction to change by crossing over two rows, i and j. (b) Another type of defect (Y) but that does not change the row stacking order in  $[1\bar{1}0]$  direction. Insets show a close up view of each defect. The scale bar and orientation vectors shown (b) are also applicable to (a). Both images were taken with biases at -2V and 50 pA.

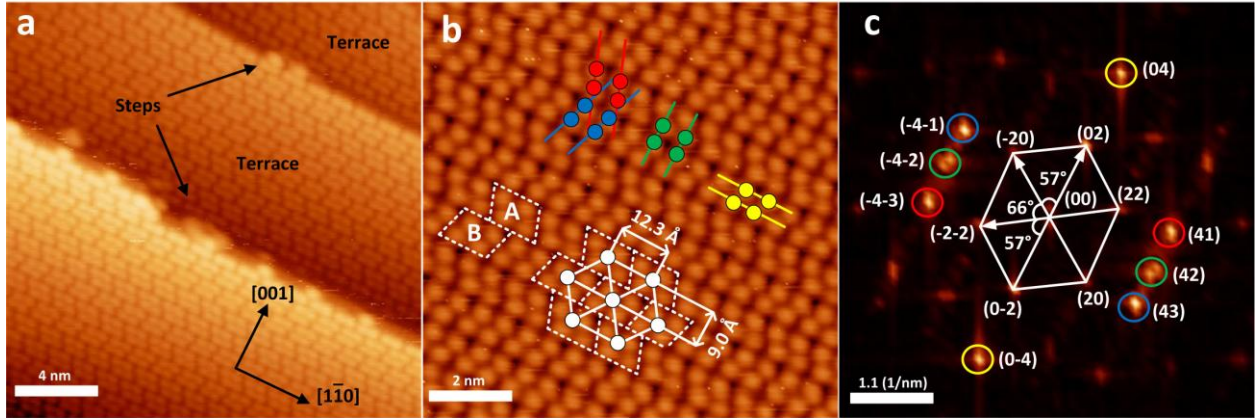




**Figure 37:** An STM image of Si(110) with several defects and noticeable rhomboid cells surface reconstruction. This substrate was the same as those in Figures 1 and 2, and was taken with biases at -2V and 50 pA.



The surface periodicities of the reconstructed Si(110) in Figure 38a-b can be analyzed with a Fourier Transform (FT), which will be compared to the unreconstructed Si(110) surface periodicities of  $\mathbf{a} \times \mathbf{b} = 5.43 \text{ \AA} \times 3.84 \text{ \AA}$  [84]. It may be noted that vector  $\mathbf{a}$  and  $\mathbf{b}$  are parallel to  $[001]$  and  $[1\bar{1}0]$ , respectively [84], which are also shown in Figure 38a as a reference. The resulting transformation in momentum space is shown in Figure 38c with indices given in the brackets. Indices (04) and (42) have periodicities of  $12.3 \text{ \AA}$  and  $9 \text{ \AA}$  and are parallel to  $[001]$  and  $[1\bar{1}0]$ , which correspond to the periodicities of the basis in Figure 37b. Therefore using the following formula  $\mathbf{a} \times (\text{periodicity of rhomboid basis in } [001] \text{ direction})$  and  $\mathbf{b} \times (\text{periodicity of rhomboid basis in } [1\bar{1}0])$ , we obtained an incommensurable  $2.3 \times 2.3$  superstructure surface reconstruction of Si(110), which is different from the  $4 \times 5$  and  $2 \times 5$  reported in Reference [85]. The superstructure can be seen with low index FT spots outlined by an oblique hexagon (in white) in Figure 38c corresponds to the real space hexagonal pattern (in white) in Figure 6.b. High order FT spots in Figure 38c are denoted with red (R), green (G), and blue (B) circles, which corresponds to the atoms in real space denoted with similar R, G, and B spheres and their respective line indices in Figure 38b.



**Figure 38:** (a) STM micrograph with biases at -2V and 50 pA of Si(110) surface after deposited with a ~1.1 nm surface coverage of Cu. (b) STM micrograph of the same Si(110) substrate with biases at -1.5V and 100 pA. Pseudo basis A and B formed hexagonal patterns with a  $2.3 \times 2.3$  superstructure. (c) Fourier transform patterns of (a) showing the corresponding the hexagonal superstructure.

#### 6.4 Summary

A long range order and incommensurable  $2.2 \times 2.3$  superstructure surface reconstruction on S(110) due to Cu was observed. The superstructure also has two different rhomboid orientations with each consisting of four atoms. The two rhomboids named A and B have the same structure but appeared to be chiral and equally distributed on the surface. Each rhomboid construction tends to be repeated along  $\langle 110 \rangle$  direction but formed a AA, BB, AB or BA stacking orders along  $\langle 001 \rangle$  direction. The rhomboid cells repeated along  $\langle 110 \rangle$  direction can be interrupted by surface defects. Nevertheless, future work is needed to determine the chemical element of the reconstructed surface.

## 7. CONCLUSIONS AND FUTURE WORK

### 7.1 Conclusions

The research presented in this thesis has focused on investigating the material properties of self assembled Cu-Si nanostructures on Si with three objectives. The first objective was to test the hypothesis that self assembled Cu-Si nanostructures would form on Si(001), Si(110), and Si(111) using e-beam evaporation in UHV. This hypothesis was successfully verified. The second objective was to characterize the material and crystallography of the self assembled Cu-Si nanostructures.  $\text{Cu}_3\text{Si}$  phase was found to be the majority phase in the Cu-Si nanostructure that were analyzed with XEDS in TEM. However, CuSi and  $\text{Cu}_3\text{Si}_7$ , which are not stable, were also found to coexist with  $\text{Cu}_3\text{Si}$ . However, we have limited information on these unstable phases since these findings were from a single nanowire on Si(001). Therefore, the non-stable Cu-Si phases could be a rare occurrence and future work on studying these unstable phases is needed.

The fabricated Cu-Si nanowires were further analyzed with TEM electron diffraction pattern to characterize their crystallographic and heteroepitaxy properties using the  $\eta\text{-Cu}_3\text{Si}$  crystal structure by Wen et al. [98]. In total, five Cu-Si nanowires were studied, i.e. two on Si(001), one on Si(111), and two on Si(110). The crystallographic orientations from this study revealed that the preferential directions of the nanowires were along  $\eta\text{-Cu}_3\text{Si}[001]$  and  $\eta\text{-Cu}_3\text{Si}[100]$ . It may be noted that the former and the latter do not belong to the same family plane. After material characterization, the thesis work focused on the third objective, which was electrical characterization. In this objective, electrical resistivity, failure current density, and density of states were investigated. The electrical resistivity and failure current density of Cu-Si nanowires were  $\sim 30 - 50 \mu\Omega\cdot\text{cm}$  and  $>1 \times 10^8 \text{ A}\cdot\text{cm}^{-2}$ , respectively. Since there was no published failure current density of Cu-Si nanowires, the data presented here are considered new. The

four and two point probe methods used in the electrical characterization require physical contact onto the Cu-Si nanowires. Thus, the nanowires would inevitably be damaged during the contact. Other surface damage of the nanowires could come from the SEM electron beam. As such, the electrical measurements have other unknown uncertainties, which are difficult to quantify and include in the error analysis.

The resistivity and failure current density, studied with four and two point probe methods, were limited to nanostructures of dimensions  $> 100$  nm. Therefore, to electrically characterize smaller nanostructures, STM was used. In this case, I-V and  $dI/dV$  spectroscopy on a sub 100 nm Cu-Si nanoisland and nanowire were measured. It was found that, at heights less than 10 nm, the Cu-Si nanostructures do not behave as metallic materials. The STM results indicate semi-metallic and semiconducting properties at this nanoscale.

While working on the thesis objectives, two unexpected results were seen on the Cu-Si samples. First, oxidation of Cu-Si nanostructures on Si(001) can produce effects similar to anisotropic etching, which forms v-channel planes along  $\text{Si}\{111\}$ . Further experiments were conducted to characterize the material properties in the nanowires during the oxidation process. The result shows that  $\text{Cu}_5\text{Si}$  ( $\kappa$  phase) was detected throughout one of the oxidized Cu-Si nanowires on Si(001). Due to the oxidation, many materials (e.g. Cu-Si,  $\text{SiO}_2$ , and Si) intermixed as identified with the TEM specimen and presented a considerable challenge to accurately characterize the composition with XEDS. In such cases, a  $\kappa\text{-Cu}_5\text{Si}$  phase was detected with a Fourier Transform (FT) image (similar to electron diffraction pattern) from a HRTEM micrograph. This is an interesting finding because  $\kappa\text{-Cu}_5\text{Si}$  phase in self assembled Cu-Si nanowires is seldom reported. However, we are uncertain whether the  $\kappa\text{-Cu}_5\text{Si}$  developed during the oxidation process or existed beforehand. The second unexpected finding was the surface reconstruction of Si(110) due to Cu deposition. Although, there was a prior study on Cu influenced Si(110) surface

reconstruction [85], the reported finding is not consistent with our results. Furthermore, our results show a long range ordered super superstructure surface reconstruction, which is rare. Most Si(110) surface reconstructions due to metal contamination as reported in References [84, 85, 124] were short range.

## 7.2 **Future Work**

Much work remains in the basic characterization of self assembled Cu-Si nanostructures using the e-beam evaporation method in UHV. The main limitation of the experimental work in this thesis is the slow progress and vast requirement of TEM work. To obtain TEM data, a completion of a sample preparation to results analysis could take up to one month, which is prohibitively long when considering only one sample was analyzed. Therefore, TEM work cannot be used for trend analysis [93] and the XEDS and electron DP in Chapter 4 has limited generalization to typical nanostructures due to the number of uncertainties in the fabrication process. Furthermore, a TEM specimen prepared by a FIB will destroy other samples as well by contaminating them with Pt particles. Therefore, in Chapter 4, the calculation of resistivity and failure current density depends on estimating the cross section area of the Cu-Si nanowires. To alleviate this issue in the future, computer simulations to assist and verify characterization of metal-silicide nanostructures are proposed.

Using advanced computer tools in tandem with TEM experimental work can expedite the research progress. For example, quantum mechanics simulations can be used to obtain electrical and electronic data such as the free electron mean path of  $\text{Cu}_3\text{Si}$  (which is presently not available) and nanoscale oxidation to verify the work in Chapter 5.

A recommended future work is to investigate the device applicability of the Cu-Si nanomaterials. The material and electrical data obtained from this thesis work can be used to assist the application of Cu-Si nanowires, e.g. resistivity modeling of electrodes in Li-Ion application [125]. However, this research

would first require a capping layer/barrier for the Cu-Si nanostructures to avoid oxidation as seen in Chapter 5. A suggested material for this capping layer graphene, which has been demonstrated to protect Ni-Si, Co-Si, and Fe-Si from oxidation [126]. Hence, a proposed future work project is to grow graphene on the Cu-Si nanostructures.

## **APPENDICES**

## APPENDIX A: LATTICE MISFIT

Lattice misfit error is calculated by using the following formula [103],

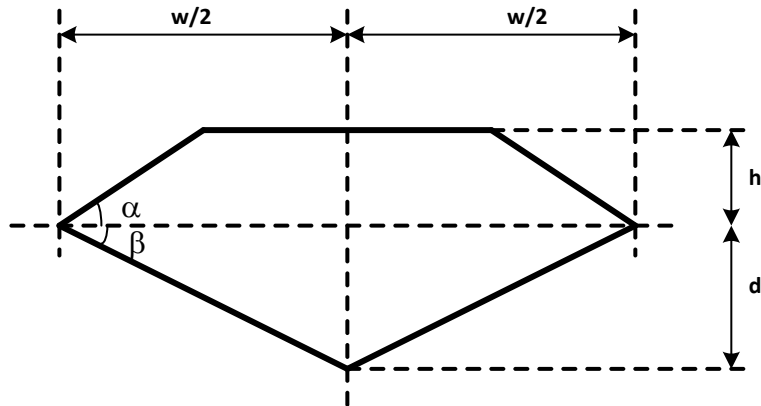
$$\text{Lattice misfit error} = \frac{A_{\text{CuSi}} - A_{\text{Si}}}{A_{\text{Si}}} \times 100\% \quad (5)$$

where  $A_{\text{Si}}$  = unstrained lattice parameters of Si (substrate) and  $A_{\text{CuSi}}$  = strained lattice parameters of  $\text{Cu}_3\text{Si}$  (epilayer).



## APPENDIX B: CROSS SECTION AREA ESTIMATION

The Cu-Si nanowires grown on Si(110) have a distinctive diamond like cross section shape (see Figure A.II.1, as seen in Figure 4.7. Assuming the geometry of a Cu-Si nanowire is proportional to its width,  $w$ , then its cross section area can be estimated. Referring to Figure A.II.1, the angles  $\alpha$  and  $\beta$  are assumed to be constants. Therefore, the ratio between  $h$  and  $w/2$  is a constant as well. Thus, we can replace  $h/(0.5w)$  with a constant  $K$ .



**Figure 39:** A cross section geometrical representation of Cu-Si nanowires on Si(110).

## APPENDIX B: CROSS SECTION AREA ESTIMATION (continued)

Hence, the cross section area in the figure can be written as below.

$$A = \frac{w^2}{2} \left( K - \frac{K^2}{2 \tan \alpha} + \frac{\tan \beta}{4} \right) \quad (\text{A.II.1}) \quad (6)$$

Using *root of the sum of the squares* [127] to perform uncertainty analysis for eq. A.II.1, we obtain the followings:

$$\Delta A = \sqrt{\left[ \Delta w \frac{\partial}{\partial w} f(w, h, \alpha, \beta) \right]^2 + \left[ \Delta K \frac{\partial}{\partial K} f(w, h, \alpha, \beta) \right]^2 + \left[ \Delta \alpha \frac{\partial}{\partial \alpha} f(w, h, \alpha, \beta) \right]^2 + \left[ \Delta \beta \frac{\partial}{\partial \beta} f(w, h, \alpha, \beta) \right]^2} \quad (7)$$

where,

$$A = f(w, h, \alpha, \beta)$$

$$\frac{\partial}{\partial w} f(w, h, \alpha, \beta) = w \left( K - \frac{K^2}{2 \tan \alpha} + \frac{\tan \beta}{4} \right)$$

$$\frac{\partial}{\partial K} f(w, h, \alpha, \beta) = w^2 \frac{1}{2} \left( 1 - \frac{K}{\tan \alpha} \right)$$

$$\frac{\partial}{\partial \alpha} f(w, h, \alpha, \beta) = w^2 \left( \frac{K}{2} \right)^2 \csc \alpha$$

$$\frac{\partial}{\partial \beta} f(w, h, \alpha, \beta) = w^2 \frac{\sec^2 \beta}{8}$$

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