

# Supporting Information: Gate Induced Carrier Delocalization in Quantum Dot Field Effect Transistors

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All electrical measurements are collected using a Keithley model 237 Source-Measure Unit to provide drain-source bias,  $V_{DS}$ , and a Keithley model 2410 Source-Measure Unit to provide gate bias,  $V_G$ , relative to the grounded source.

## Room temperature Mobility

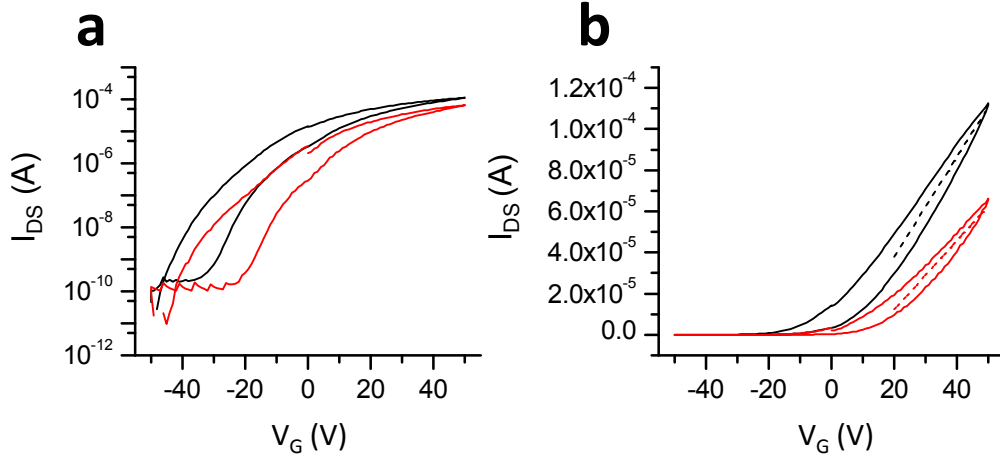


Figure S1:  $I_{DS}$  vs  $V_G$  with  $I_{DS}$  plotted (a) logarithmically and (b) linearly for two measurements taken at different times on our sample during the course of our study (black and red). Dashed lines are fits used to calculate mobilities of Measurement 1 (black,  $12 \text{ cm}^2/\text{Vs}$ ) and Measurement 2 (red,  $8 \text{ cm}^2/\text{Vs}$ ).

Room temperature  $I$  vs  $V_G$  curves used to calculate the sample mobility,  $\mu$ , are shown in Figure S1. Mobility is calculated in the linear region using

$$I_{DS} = C_i \mu \frac{W}{L} (V_G - V_T) V_{DS} \quad (\text{S1})$$

where  $C_i$  is the capacitance per unit area, calculated to be  $13.3 \text{ nF}/\text{cm}^2$  using  $\kappa = 3.9$  for  $\text{SiO}_2$  and  $\kappa = 9$  for  $\text{Al}_2\text{O}_3$ ,<sup>1</sup>  $W = 600 \text{ }\mu\text{m}$  is the channel width,  $L = 40 \text{ }\mu\text{m}$  is the channel length,  $V_G$  is the gate bias,  $V_T$  is the threshold bias, and  $V_{DS} = 1 \text{ V}$  is the drain-source bias used to collect the data in Figure S1.<sup>2</sup>

## Analysis of the Reduced Activation Energy

For samples with a resistance  $R$  of the form  $R(T) = R_0 \exp(T_0/T)^p$  with temperature  $T$ , the reduced activation energy  $W$  can be used to extract  $p$  and  $T_0$  objectively.

$$W \equiv -\frac{d \ln R}{d \ln T} \quad (\text{S2})$$

$$= p \left( \frac{T_0}{T} \right)^p \quad (\text{S3})$$

$$\log W = \log(p(T_0)^p) - p \log T \quad (\text{S4})$$

A plot of resistance,  $R$  vs  $T^{-1/2}$  is shown in Figure S2a to demonstrate the relatively poor match of this data to  $p = 1/2$ . A plot of  $\log W$  vs  $\log T$  is shown in Figure S2b with extracted values for  $T_0$  and  $p$ .

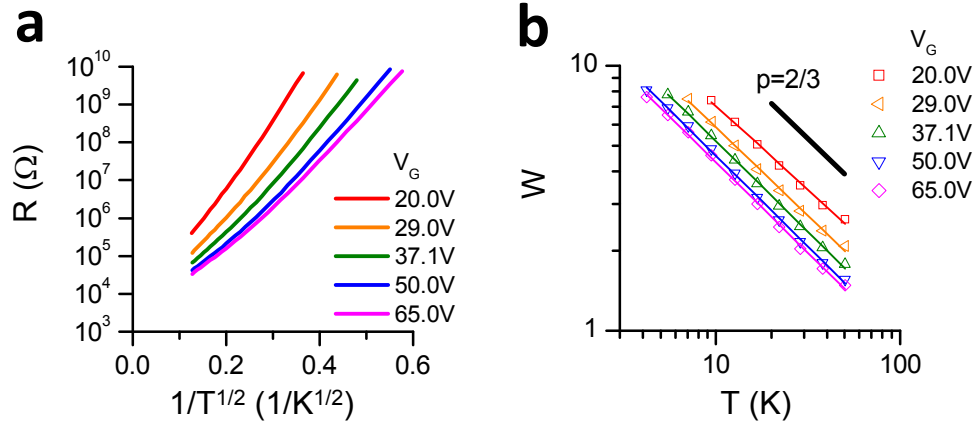


Figure S2: (a) Resistance,  $R$ , vs.  $T^{-1/2}$  for different  $V_G$ . (b) Reduced activation energy  $W = -\frac{d \ln R}{d \ln T}$  vs.  $T$  for a QD FET at  $V_G = 65$  V. Lines indicate fits to the data yielding  $p$  equal to 0.63, 0.66, 0.68, 0.69 and 0.68 for  $V_G = 20.0, 29.0, 37.1, 50.0$  and  $65.0$  V, respectively.

## Bias Dependence

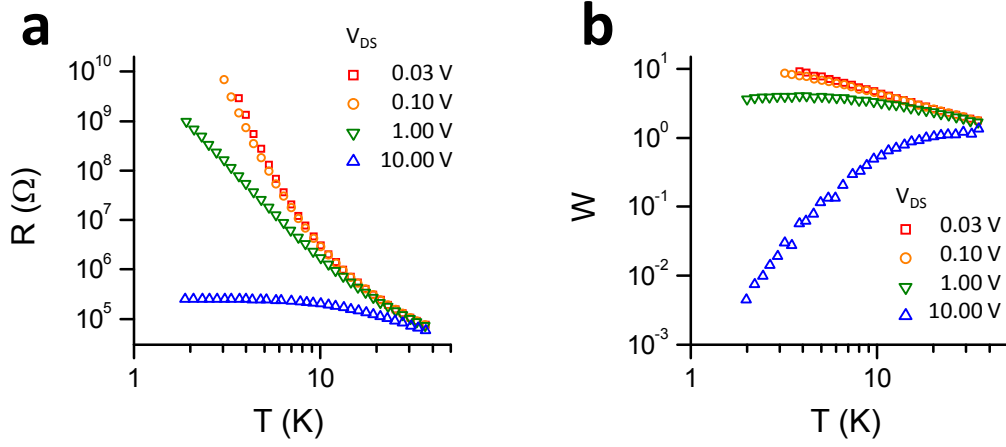


Figure S3: Drain-source bias dependence of (a) resistance and (b) reduced activation energy  $W = -\frac{d \ln R}{d \ln T}$  vs temperature for a QD FET at  $V_G = 65V$ .

As shown in Figure S3, the measured  $R(T)$  and  $W(T)$  depend strongly on the applied drain-source bias of the sample. At high  $V_{DS}$  and low temperature electric field activation of carriers dominates thermal activation.

Warming curves shown in the main text were taken at  $V_{DS}=0.1$  V. Leakage measurements between source/drain and gate electrode were acquired at  $V_{DS}=0.0001$  V and subtracted from the warming curve to increase fidelity at low temperatures where the leakage current dominates. Curves are truncated when the drain-source current drops below  $10^{-11}$  A which occurs before  $I_{GS} > 0.1 I_{DS}$ .

## Dielectric constant

Figure S4 shows the dielectric constant  $\kappa$  as measured in ellipsometry. Figure S5 shows the implied changes to the dielectric constant  $\kappa$  if the localization length were to remain unchanged with applied gate bias.

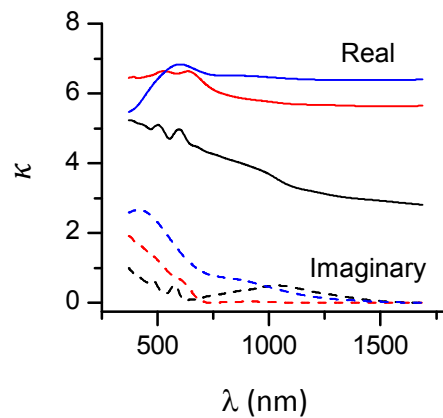


Figure S4: Measured dielectric constant from ellipsometry. Black: as-deposited, red: annealed without indium at 250 °C, blue: annealed with indium at 250 °C.

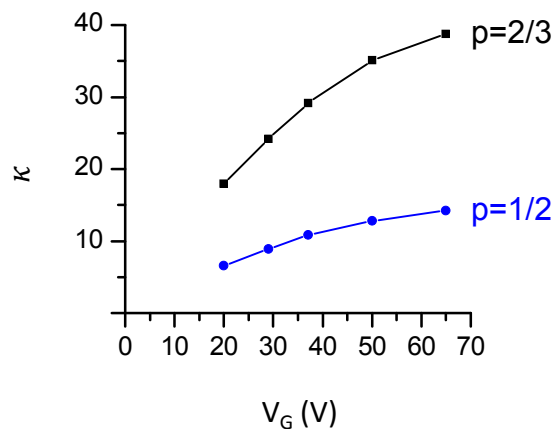


Figure S5: Dielectric constant  $\kappa$  that results if the localization length  $a$  is held fixed at the QD diameter.

## Magnetoresistance Measurements

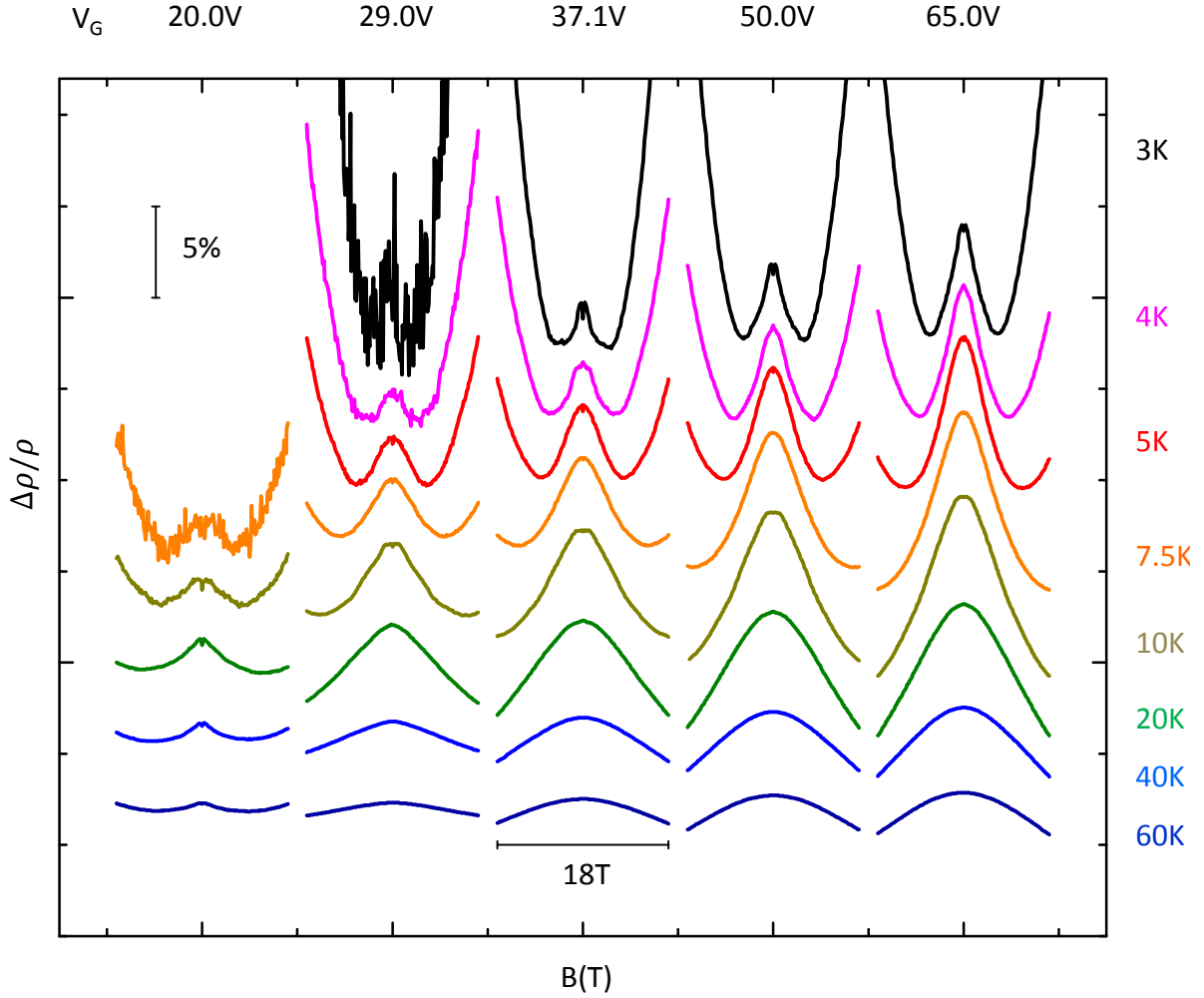


Figure S6: Magnetoresistance (MR) of a QD FET *vs.* applied gate bias  $V_G$  and temperature  $T$ . Plots are vertically and horizontally offset for clarity.

All magnetoresistance curves used for temperature-based decomposition of MR features are shown in Figure S6.

MR at  $V_G = 20V$  maintained the presence of a positive high-field feature for all temperatures measured and was resultantly not used in the scaling analysis shown in the body text. For temperatures below 7.5K,  $V_G = 20V$  MR is not shown because the signal to noise ratio is insufficient.

## References

- (1) Robertson, J. *Eur. Phys. J.: Appl. Phys.* **2004**, *28*, 265–291.
- (2) Horowitz, G. *Adv. Mater.* **1998**, *10*, 365–377.