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# Solutions Manual – Introduction to Flexible Electronics

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**2.1. Consider a glass substrate which needs to be flexed up to the bending radius of 5 cm.**

**We require the substrate to be a 2 cm x 2 cm square piece. Given the fracture stress of glass is 70 MPa and Young’s modulus is 70 GPa, what should be the thickness of the substrate?**

**Ans:** Stress= 70 MPa

Young’s modulus= 70 GPa

Bending radius= 5 cm

$$Young's\ Modulus = \frac{Stress}{Strain}$$

$$Strain = \frac{Stress}{Y}$$

$$Strain = \frac{70 * 10^6}{70 * 10^9} = 10^{-3}$$

$$Strain = \frac{t}{2R}$$

$$Thickness\ (t) = 10^{-3} * 2 * 0.05$$

$$Thickness = 10^{-4}m = 0.1\ mm$$

**2.2. We have a chain of  $n$  atoms of radius  $r$  bonded together by a chemical bond. The bond is approximated as a spring of constant  $k$  (N/m). What is the young's modulus of this material chain along the axis of bonding?**

**Ans:** Young's modulus,  $Y = \frac{\text{Stress}}{\text{Strain}}$

$$Y = \frac{\frac{F}{A}}{\frac{\Delta L}{L}}$$

$$Y = \frac{FL}{A \Delta L}$$

*By Hooke's Law, since  $F = kx$*

$$Y = \frac{kL}{A}$$

$$\text{Therefore, } Y = \frac{kL}{n\pi r^2}$$

**2.3. Consider a square plate of size 5 cm x 5 cm and thickness of 0.1 mm. The Young's modulus of the material is 1 GPa and the Poisson's ratio is 0.4. Calculate the flexural rigidity in the direction normal to the thickness. What is the minimum horizontal force required to buckle this plate?**

**Ans:** Flexural rigidity,  $D = \frac{Eh^3}{12*(1-\nu^2)}$

$$D = \frac{10^9 * (0.1 * 10^{-3})^3}{12 * (1 - 0.4^2)}$$

$$D = \frac{10^{-3}}{10.08}$$

$$D = 9.92 * 10^{-5}$$

Minimum horizontal force =  $N_c = \frac{\pi^2 D}{L^2}$

$$N_c = (3.14^2 * 9.92 * 10^{-5}) / (10^{-8})$$

$$N_c = 9.78 * 10^4 \text{ N}$$

**2.4. For the plate in question 2.3, obtain the moment of force required to flex the plate to the bending radius of 20 cm.**

**Ans:** Moment of force,  $M = \frac{D}{R}$

$$M = \frac{9.92 * 10^{-5}}{0.2}$$

$$M = 4.96 * 10^{-6} \text{ N-m}$$

**2.5. Obtain equation for the curvature for the curve  $y = ax^n$  at the origin, where  $a$  and  $n$  are constants.**

**Ans:**

$$k = \frac{|y''|}{(1+y'^2)^{3/2}}$$

$$y = ax^n$$

$$y' = anx^{n-1}$$

$$y'' = an(n-1)x^{n-2}$$

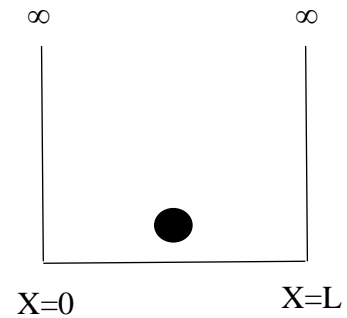
$$k = \frac{|an(n-1)x^{n-2}|}{(1+(anx^{n-1})^2)^{3/2}}$$

At origin (0,0)

$$k = 0$$

**3.1. Consider a particle of mass 1 gram in an infinite 1D potential well of 1 cm length. Obtain an expression for the allowed energy levels for the particle, in terms of the quantum number,  $n$ . Assume that the particle has 1 Joule energy. Which energy level will it occupy? Calculate the difference in energy between this and the next higher energy allowed level.**

**Ans:**



The potential energy is 0 inside the box ( $V=0$  for  $0 < x < L$ ) and goes to infinity at the walls of the box ( $V=\infty$  for  $x < 0$  or  $x > L$ ). The time-independent Schrödinger equation for a particle of mass  $m$  moving in one direction with energy  $E$  is

$$-\frac{\hbar^2}{2m} \frac{d^2\psi(x)}{dx^2} + V(x)\psi(x) = E\psi(x)$$

- $\hbar$  is the reduced Planck constant where  $\hbar = h/2\pi$
- $m$  is the mass of the particle
- $\psi(x)$  is the stationary time-independent wavefunction
- $V(x)$  is the potential energy as a function of position
- $E$  is the energy, a real number

This equation can be modified for a particle of mass  $m$  free to move parallel to the  $x$ -axis with zero potential energy ( $V = 0$  everywhere) resulting in the quantum mechanical description of free motion in one dimension:

$$-\frac{\hbar^2}{2m} \frac{d^2\psi(x)}{dx^2} = E\psi(x)$$

This equation has been well studied and gives a general solution of:

$$\psi(x) = A\sin kx + B\cos kx$$

where A, B, and k are constants.

According to our boundary conditions, the probability of finding the particle at  $x=0$  or  $x=L$  is zero. When  $x=0$ , then  $\sin(0)=0$  and  $\cos(0)=1$ ; therefore,  $B=0$  to fulfill this boundary condition giving:

$$\psi(x) = A\sin kx$$

For  $\psi(L)=0$

$$A\sin kL = 0$$

$$\sin kL = 0$$

$$kL = n\pi$$

$$k_n = \frac{n\pi}{L}$$

$$k = \sqrt{\frac{2m_0E}{\hbar^2}}$$

$$\text{Therefore, } \psi_n(x) = \sqrt{\frac{2}{L}} \sin \frac{n\pi x}{L}$$

$$\text{Hence, } E = \frac{\hbar^2 n^2 \pi^2}{2m_0 L^2}$$

The allowed energy levels are,  $E = \frac{h^2 n^2}{8m_0 L^2}$



For particle of mass  $m$  gram and length 1 cm for 1 J of energy, the level it will occupy will be

$$n = \sqrt{\frac{8EmL^2}{h^2}}$$

$$n = 1.35 * 10^{30}$$

The difference between this and the next energy level can be approximated as:

$$E = \frac{h^2 n^2}{8m_0 L^2}$$

$$dE = \frac{h^2 n}{4m_0 L^2}$$

$$dE = 1.47 * 10^{-30} J$$

**3.2. The bandgap of silicon is 1.1 eV and the Fermi level is midway between the valence and conduction band. What is the probability of occupation of the valence and conduction band edge at room temperature (300 K)?**

**Ans:**

$$f(E) = \frac{1}{1 + e^{\frac{E-E_F}{KT}}} = e^{-\left(\frac{E-E_F}{KT}\right)}$$

For occupancy in conduction band,

$$E = E_c$$

$$E_F = \frac{(E_C + E_V)}{2}$$

$$E_C - E_F = \frac{(E_C - E_V)}{2} = \frac{E_G}{2}$$

So the probability is  $f(E_c) = e^{-\left(\frac{E_G}{2KT}\right)}$

$$E_G = 1.1 \text{ eV}$$

$$KT = 0.026 \text{ eV}$$

$$f(E_c) = 6.526 * 10^{-10}$$

**3.3. Describe the process steps involved in obtaining silicon crystal silicon ingots from silicon ore quartzite.**

**Ans:** Quartzite is silicon dioxide with trace amounts of iron and other contaminant oxides.

1. High purity quartzite is reduced to silicon using coke at high temperatures. Generally, an excess of quartzite is maintained to limit the formation of silicon carbide.
2. The resulting silicon is only around 98% pure and thus has to be purified before being made into silicon chips.
3. The purification process is based on the distillation of trichlorosilane ( $\text{SiHCl}_3$ ) and is known as the Siemen's process.
4. Powdered silicon is reacted with hydrochloric acid ( $\text{HCl}$ ) to form  $\text{SiHCl}_3$ , which has a low boiling point of  $31.8^\circ\text{C}$ .
5. The  $\text{SiHCl}_3$  vapor is distilled and is reduced to pure silicon using hydrogen gas.
6. Several iterations of the Siemen's process lead to ultra-pure silicon, known as electronic-grade silicon. The purity of this silicon is approximately 99.999998%

A crystalline silicon ingot is obtained from the electronic grade silicon using the Czochralski (CZ) process.

1. The silicon is melted in a quartz crucible and is recrystallized according to a seed crystal structure.
2. The seed crystal is dipped into the silicon melt and pulled out of the melt, giving a crystalline ingot.
3. The cylindrical ingot is then cut into individual silicon wafers.
4. In case a silicon wafer with a particular dopant concentration is required, an appropriate amount of dopant element can be added to the melt.
5. The silicon wafers thus obtained have very high purity and crystalline integrity.

**3.4. What are the advantages and disadvantages of E-beam lithography over conventional UV photolithography?**

**Ans:** Advantages:

1. They have much lower wavelength compared to UV photolithography.
2. They have better resolution capabilities.

Disadvantages:

1. It has low throughput because it can expose a single point on the substrate at a time, as opposed to the flood exposure feature of UV radiation.

**3.5. Assume that a wet etch has a time-dependent vertical etch rate of  $r_v(t) = \frac{k}{t+\tau}$  nm/s, where  $\tau$  and  $k$  are constants with units of time and distance, respectively. What is the time taken to etch through a thin film of thickness  $2k$ ? If the anisotropy of the etch has to follow the equation  $A = e^{-t/\tau}$ , what should be the horizontal etch rate as a function of time?**

**Ans:**

$$r_v(t) = \frac{k}{t+\tau}$$

We know that,

$$r_v(t) = \frac{\partial d_v}{\partial t}$$

$$d_v = \int \frac{k}{t+\tau} \partial t$$

$$d_v = k[\ln(t+\tau) + c]$$

$$2k = k[\ln(t+\tau) + c]$$

$$t + \tau = e^{2-c}$$

$$t = e^{2-c} - \tau$$

To find horizontal etch rate , we know that

$$A = 1 - \frac{r_h}{r_v}$$

$$r_h = (1 - A) * r_v$$

$$r_h = \frac{k}{t+\tau} (1 - e^{-\frac{t}{\tau}})$$

**4.1. What is an SOI substrate? What are the processes used to fabricate SOI substrates starting with bulk silicon substrates?**

**Ans:** The SOI substrate consists of a thin layer of single-crystal silicon on a layer of silicon dioxide, attached to a handle silicon substrate. The thickness of the top silicon varies from a few nanometres (3 nm) in the case of ultra-thin body SOI (UTBSOI) to 30  $\mu\text{m}$ , depending on the fabrication process and the intended application.

The following are the processes used to fabricate SOI substrates:

1. SIMOX process: This was one of the first processes used to obtain SOI substrates. In this method, oxygen atoms are implanted into a regular silicon wafer at the desired depth. This is followed by annealing to form bonds between silicon and oxygen leading to a buried silicon oxide layer. The depth of the buried oxide can be controlled using the implantation energy of oxygen ions, and the thickness of the layer can be controlled using the amount of oxygen implanted (or the implantation dose) due to which it suffers surface damage due to the impact of higher energy ions. Because this is also the surface to be used for device formation, it is critical to recover this damage. One of the ways in which this can be done is using the epitaxy process. It is a specialized CVD process in which the deposition is carried out to form a single-crystal layer following the template of a seed layer. An epitaxial layer of silicon is grown using the damaged silicon as a template to hide the vacancy and other defects at the surface of the wafer. However, the defect density of the top surface is still higher than that of bulk silicon (100) wafers.
2. Smart Cut process: In this process, hydrogen ions are implanted into an oxidized silicon wafer. The wafer is then bonded with another silicon substrate. When this structure is annealed, the hydrogen ions congregate to form microbubbles that cause the silicon substrate to split. The bonded silicon substrate then has an oxide layer and a silicon layer attached to it. The top layer is polished to create a pristine surface for electronic

device formation. The thickness of the top silicon is again controlled using the implantation energy, while the thickness of the buried oxide is controlled through the oxidation of the initial silicon wafer. A key advantage of this process is the use of hydrogen ion implantation instead of oxygen ions. Because of the small size and mass of hydrogen ions, the lattice damage due to implantation is significantly lower in the Smart Cut process compared to the SIMOX process. However, this process makes the resultant SOI substrate more expensive because of the use of two silicon wafers to fabricate one SOI substrate.

3. The bond-and-etch-back SOI (BESOI) process: In this process, two silicon wafers (one of them oxidized) are bonded, followed by the back etching of one of the substrates. The etch-back and polish are used to control the thickness of the final top silicon, while the thickness of the buried oxide is controlled through oxidation of the initial silicon wafer. An advantage of this process is that it avoids the implantation process altogether, thus reducing the damage to the silicon surface. However, the etch-back is hard to control precisely over the large silicon surface, which can lead to an inconsistent thickness of the top silicon layer.

**4.2. List the advantages of the TPER process for fabricating flexible silicon from bulk silicon substrates, post-device fabrication. What are the disadvantages?**

**Ans:**

Advantages:

1. It is a device-first process, thus high-performance state-of-the-art circuits can be fabricated before they are flexed using this process.
2. The steps involved in the process do not subject the wafer to high temperatures or high thermal budgets because circuits have already been fabricated on the wafer, it likely consists of millions of transistors, p-n junctions and metal interconnects before being subjected to the TPER process. These components are temperature sensitive and can be damaged irreparably if the wafer is subjected to high temperature or thermal budget. The highest temperature in the TPER process is the ALD deposition of aluminium oxide. This step can be carried out at a temperature of sub-100°C, which is an acceptable temperature for silicon wafers, post-circuit fabrication. Thus, the performance of the prefabricated circuit does not degrade due to the TPER process.
3. The process steps involved in the TPER process are compatible with CMOS fabrication technology. The materials, chemicals, tools, and techniques used in the process are already used in many steps involved in the CMOS fabrication process. Thus, the fabrication facility adopting the TPER process to fabricate flexible silicon circuits will not need additional tooling or infrastructure to carry out the process once the circuit fabrication is complete.
4. The TPER process affords a high degree of control over the thickness of the top silicon released. This is achieved by varying the depth of the trenches inside silicon, which, in turn, can be controlled by changing the number of cycles of the DRIE process. It should be noted that the thickness of the released silicon is lower than the depth of the trench because the isotropic etch of silicon also progresses vertically upward.



5. In this process, the silicon substrate remaining after removal of the top silicon surface can be reused after polishing. The typical thickness of a silicon wafer is 0.5 mm. If the top 0.1 mm is lost during the release process, the remaining 0.4 mm silicon substrate can be polished and reused as normal.
6. The flexible silicon piece resulting from the TPER process has uniformly distributed microscopic through-holes throughout the silicon surface. This gives the silicon piece a semi-transparent characteristic. It has a transmittance of around 7% in the visible light region. This can be used for heat dissipation or for fabrication of through silicon vias (TSVs) for 3D integration of flexible silicon pieces.

Disadvantages:

1. A key disadvantage is the loss of the silicon area because of the placement of trenches on the silicon floor. These trenches are made after the completion of the circuit and metal interconnect fabrication; thus, their placement can place a major constraint on the placement and routing of the silicon circuit. On average, these holes consume about 20% of the silicon floor in most of the flexible devices reported in the literature.
2. Due to the inter-device separation being very small in modern state-of-the-art devices, there will be a constraint on the size of the trenches that can be placed there. This will limit the depth of the trenches because DRIE processes can only provide a certain aspect ratio of trenching. This, in turn, will limit the thickness of the final flexible silicon piece obtained using this process. Thus, some loss of silicon real estate may be unavoidable if the TPER process is used.
3. It produces flexible silicon pieces with semi-spherical “scallop” at the bottom. These are caused because the etch bubbles of the isotropic etch progress at the same rate in all directions, including upward from the bottom of the trench. This causes more silicon to be removed near the trench bottom compared to other areas, leading to the formation of

scallops. This uneven surface finish can cause problems when the flexible silicon pieces are transferred onto a flat surface.

4. While bending, the flexural stress may be distributed unevenly because of these structures, which may lead to cracking or fracture of the silicon pieces even before the minimum bending radius is achieved. However, this effect can be mitigated by creating thinner-than-required flexible silicon pieces so that the increased flexural stress can be adjusted against the lower flexural rigidity to obtain a specific bending radius.

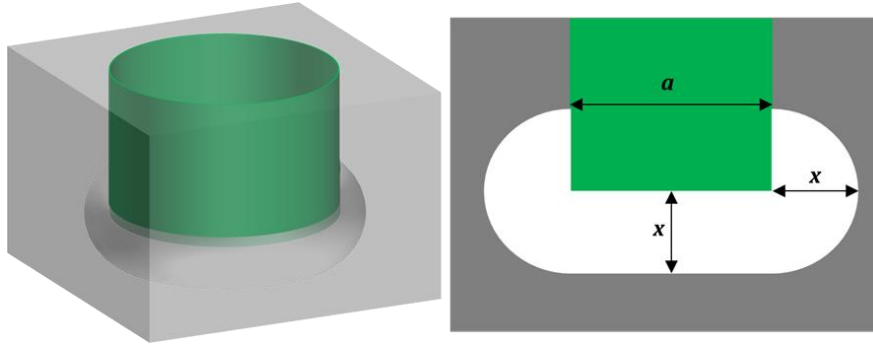
**4.3. Compare the four processes for bottom-up device-first approach – 1. Back grinding, 2. CMP, 3. Wet etching, 4. Soft back etch – in terms of speed, stress on the wafer, and TTV obtained.**

**Ans:**

	Speed	Stress on the wafer	TTV obtained
Back grinding	Fast	High	High
CMP	Slow	Low	Less
Wet etching	Slow	Least	Less
Soft back etch	Slow	Least	Less

**4.4. Consider the use of the TPER process to create flexible silicon circuits using an SOI substrate. We create circular trenches with 10  $\mu\text{m}$  diameter, with their centers on a square lattice of 20  $\mu\text{m}$  side. If one cycle of  $\text{XeF}_2$  etch removes  $n$  moles of silicon, how many cycles are required to flex the SOI piece?**

**Ans:**



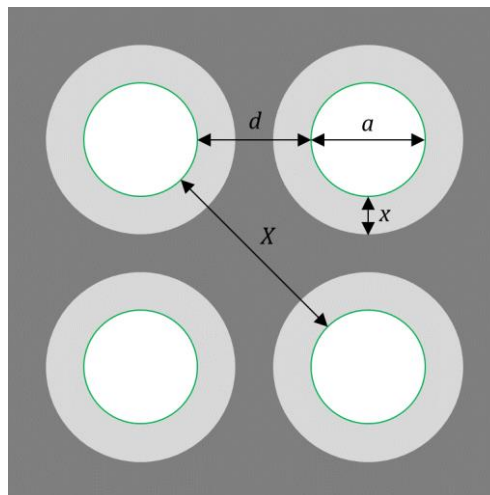
If the diameter of the etch cylinder is  $a$ , the volume of the etched material at any time can be given by the sum of the volumes of the cylinder and semi-toroid as:

$$V = \frac{\pi^2 a x^2}{4} + \frac{\pi a^2 x}{4}$$

$$V = \frac{\pi a x}{4} (\pi x + a)$$

As the etch goes on, the value of  $x$  increases. When the etch toroids from the adjacent trenches meet, the release of the silicon top layer is completed. Now, consider the distance between adjacent trenches to be  $d$ . Hence, from Figure 2, the value of  $x$  for a just completed etch can be obtained as:

$$X = \sqrt{2}(d + a) - a$$



Hence, the volume per trench needed to etch for a just completed silicon release is given by:

$$V = \left(\frac{1}{4}\right) (\pi a [\sqrt{2}(d + a) - a]) (\pi [\sqrt{2}(d + a) - a] + a)$$

This equation, completely dependent on the trench geometry, describes the volume of silicon to be etch for a completed release. The number of moles required to be etched are:

$$N = \frac{V\rho}{N_a}$$

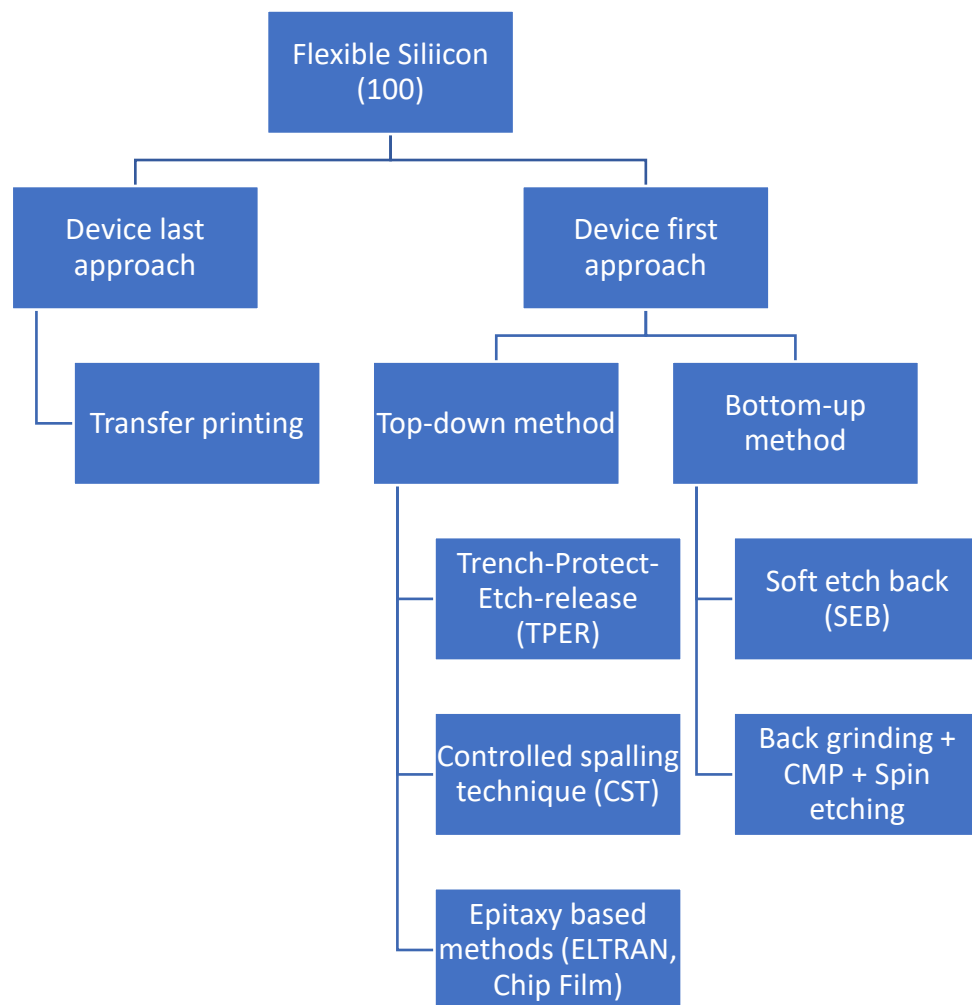
Where  $N_a$  is the Avogadro's constant. Thus, the number of cycles of  $\text{XeF}_2$  required are  $N/n$ .

**4.5. Name all the key methods that can be used to create flexible monocrystalline silicon. Mention their advantages/disadvantages in brief. Draw a tree indicating the classifications of all the methods.**

**Ans:**

The key methods that can be used to create flexible monocrystalline silicon are:

1. Transfer printing
2. Trench-Protect-Etch-release (TPER)
3. Controlled spalling technique (CST)
4. Epitaxy based methods (ELTRAN, Chip Film)
5. Soft etch back (SEB)
6. Back grinding + CMP + Spin etching



## 1. Transfer printing

### Advantages:

- a. The transfer process can be performed at room temperature and pressure using inexpensive equipment and materials.
- b. As the silicon pieces are bonded to the destination substrates early in the circuit fabrication process, the integration of silicon-based devices with other types of electronics (like organic electronics) is easier using this technique.
- c. The process is very versatile and can be used to transfer silicon pieces of any shape and size.

### Disadvantages:

- a. The reactant species such as the hydrogen and fluoride ions need to travel across the silicon piece to be undercut to reach the last remaining oxide support while the reaction products need to be ejected out in the other direction. This causes a gradient in the concentration of reaction species causing a slowing of the etching rate as the etch progresses. Thus, reaction time increases exponentially with the size of silicon pieces to be released.
- b. Since, the edges of the silicon pieces are unsupported during the reaction, a section of the piece, if sufficiently large, can sag and stick to the silicon handle substrate. This may cause the transport of reaction species to completely stop, thus putting a limit on the size of the silicon piece that can be successfully undercut using lateral etching of SOI substrates.
- c. The cost of the process is increased because a percentage of the top silicon surface is lost to etching.
- d. There are several steps remaining in the process of converting the silicon pieces into working MOS devices. After the transfer printing, these steps must be

completed while the silicon pieces are attached to a flexible substrate. This limits the temperature and overall thermal budget the follow up processes can afford which might lead to a sub-optimal final device.

- e. Another challenge in processing the transferred flexible silicon pieces is that most semiconductor fabrication tools are designed for rigid substrates and cannot be used directly on flexible substrates without rigid support. This makes the processing more complicated and time-consuming.

## 2. TPER Process:

### Advantages:

- a. It is a device-first process, thus high-performance state-of-the-art circuits can be fabricated before they are flexed using this process.
- b. The steps involved in the process do not subject the wafer to high temperatures or high thermal budgets because circuits have already been fabricated on the wafer, it likely consists of millions of transistors, p-n junctions and metal interconnects before being subjected to the TPER process. These components are temperature sensitive and can be damaged irreparably if the wafer is subjected to high temperature or thermal budget. The highest temperature in the TPER process is the ALD deposition of aluminium oxide. This step can be carried out at a temperature of sub-100°C, which is an acceptable temperature for silicon wafers, post-circuit fabrication. Thus, the performance of the prefabricated circuit does not degrade due to the TPER process.
- c. The process steps involved in the TPER process are compatible with CMOS fabrication technology. The materials, chemicals, tools, and techniques used in the process are already used in many steps involved in the CMOS fabrication process. Thus, the fabrication facility adopting the TPER process to fabricate flexible silicon circuits will not need additional tooling or infrastructure to carry out the process once the circuit



fabrication is complete.

- d. The TPER process affords a high degree of control over the thickness of the top silicon released. This is achieved by varying the depth of the trenches inside silicon, which, in turn, can be controlled by changing the number of cycles of the DRIE process. It should be noted that the thickness of the released silicon is lower than the depth of the trench because the isotropic etch of silicon also progresses vertically upward.
- e. In this process, the silicon substrate remaining after removal of the top silicon surface can be reused after polishing. The typical thickness of a silicon wafer is 0.5 mm. If the top 0.1 mm is lost during the release process, the remaining 0.4 mm silicon substrate can be polished and reused as normal.
- f. The flexible silicon piece resulting from the TPER process has uniformly distributed microscopic through-holes throughout the silicon surface. This gives the silicon piece a semi-transparent characteristic. It has a transmittance of around 7% in the visible light region. This can be used for heat dissipation or for fabrication of through silicon vias (TSVs) for 3D integration of flexible silicon pieces.

Disadvantages:

- a. A key disadvantage is the loss of the silicon area because of the placement of trenches on the silicon floor. These trenches are made after the completion of the circuit and metal interconnect fabrication; thus, their placement can place a major constraint on the placement and routing of the silicon circuit. On average, these holes consume about 20% of the silicon floor in most of the flexible devices reported in the literature.
- b. Due to the inter-device separation being very small in modern state-of-the-art devices, there will be a constraint on the size of the trenches that can be placed there. This will limit the depth of the trenches because DRIE processes can only provide a certain aspect ratio of trenching. This, in turn, will limit the thickness of the final flexible silicon piece

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### 3. CST:

Advantages:

- a. This process can obtain flexible silicon chips of precise thickness without the loss of silicon material (say in lateral etching).
- b. The materials and processes used in this technique are compatible with CMOS fabrication processes, thus, can be included in the process flow for flexible silicon chip fabrication.

Disadvantages:

- a. The stress induced in the silicon because of the stressor layer can change the charge transport properties of the lattice.
- b. The change in lattice properties affects these transistor types differently, thus causing a mismatch in the CMOS circuits. This can change the performance of the circuit if it is not accounted for at the circuit design stage

- c. The uneven distribution of stress inside the lattice can cause the circuit to malfunction.

### 4. Epitaxy based methods (Chip Film)

Advantages:

This process supports state-of-the-art CMOS circuits (being a device-first approach), and

being CMOS fabrication compatible, providing thickness control (through thicknesses of fine porous silicon and epitaxial silicon layer), having a pick-and-place strategy in-built into the process, and having a smooth bottom finish for flexible silicon chips.

Disadvantages:

Silicon wafers are subjected to the complete CMOS fabrication cycle with the large under surface cavities in place, which may lead to increased surface roughness and tightening of the process window in some steps. Further, the technology entails implementing an extensive pre-fabrication module, including an epitaxy process step, which can reduce throughput and add to the cost of the chips.

#### 5. Soft etch back (SEB)

Advantages:

The top surface of the wafer is protected using a thick layer of photoresist.

Disadvantages:

There can be variations in the etch depth depending on the design of the chamber and the substrate loading. Because a significant percentage of the substrate needs to be etched, it is difficult to stop the etch at the precise time to obtain a specific thickness of silicon. Thus, this process is ideally used in the presence of an etch stop layer such as the buried oxide in the case of circuits fabricated on the SOI substrate.

#### 6. Back grinding + CMP + Spin etching

Advantages and Disadvantages:

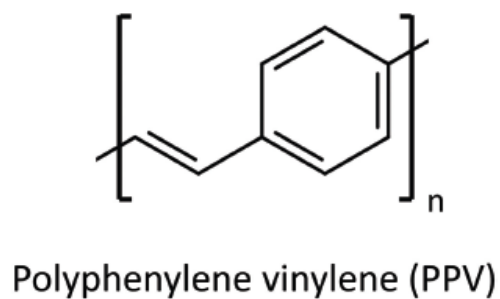
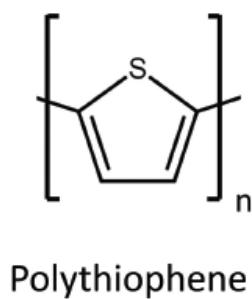
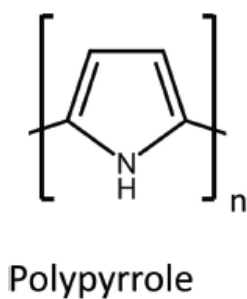
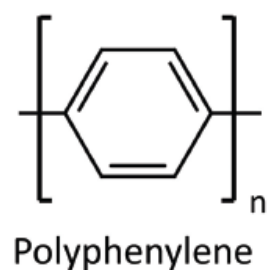
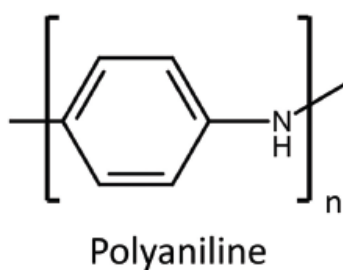
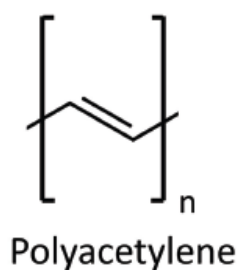
While back-grind is fast and cheap, it can cause substrate damage.

CMP and chemical etching are relatively low stress but are slow and expensive.

**5.1. Draw the conjugated  $\pi$ -bond structure for the following organic polymers:**

- a. Polyacetylene
- b. Polyaniline
- c. Polyphenylene
- d. Polypyrrole
- e. Polythiophene
- f. Poly(p-phenylene vinylene)

**Ans:**



**5.2. State the key differences in electronic conduction properties of organic electronic materials compared to their inorganic counterparts.**

**Ans:** In inorganic components such as silicon, the individual atoms, even if they are of a highly conductive elements like silver, are not conductive on their own or as a collection. Electrical conductivity only arises in these lattices when multiple atoms come together in such a way that allowed energy states for electrons are shared across the lattice and electrons in these energy states can travel across the lattice. The probability of the existence of electrons at a particular point in the lattice and the distribution of their velocities then depend not only on the internal distribution of charged nuclei but also on external factors such as applied electromotive force. This phenomenon is referred to as electrical conductivity. In inorganic lattices, the shared energy states across the lattice, obtained because of the specific distribution of potential wells (nuclei), give rise to the observed electrical conductivity.

In case of, organic molecules, the electrons associated with the molecules are tightly held in carbon-carbon bonding orbitals. Again, these molecular orbitals arise because of the solution to the distribution of electrons according to the potential wells of the nuclei of carbon atoms and other atoms participating in the molecule. These solutions permit electrons to have energy levels lower than those in the individual atoms (thus leading to a stable molecule). These molecular orbitals are called “bonding” orbitals. Electrons in bonding orbitals have a high probability of being between the two nuclei participating in the bond. The complete solution to the electron distribution within the molecule also results in higher energy molecular orbitals. These orbitals may permit electrons to have shared energy states across the molecule where intramolecular conduction may be possible, however, the energy of these “anti-bonding” molecular orbitals is very high for any practical conduction to take place.

**5.3. Why are organic materials better suited for the fabrication of LEDs compared to photovoltaics?**

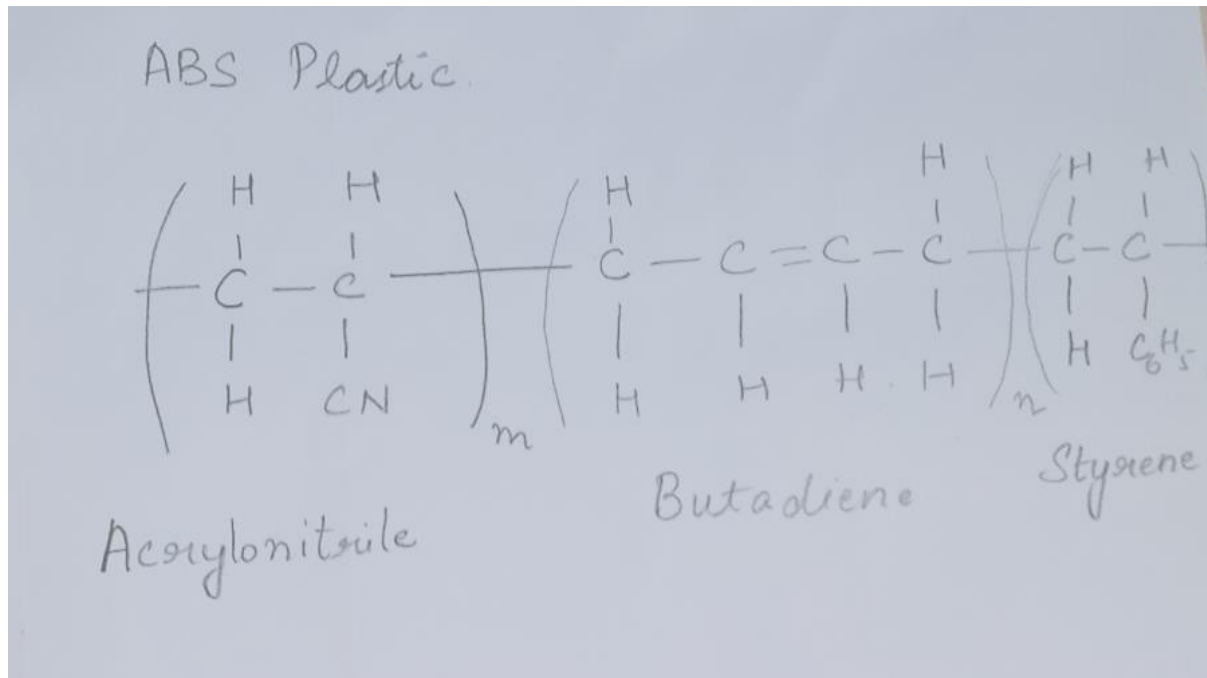
**Ans:** Organic materials are better suited for the fabrication of LEDs compared to photovoltaics because electron-hole pairs in organic materials have a higher binding energy. Hence, electrons and holes are more likely to recombine and form a photon. In case of photovoltaics, it is desirable that, once created, electron-hole pairs are separated for current conduction. This is more likely in inorganic materials, where the binding energy is smaller.

**5.4. What is one method of fabricating organic field-effect transistors without exposing the organic material to the fabrication process steps?**

**Ans:** The fabrication of organic FETs using organic crystals is the use of silicon or plastic substrate for metal contact and dielectric layer formation. In this method, the source/drain contact and dielectric layer are deposited and patterned on silicon or plastic substrate using standard thin-film processing techniques. The organic single crystal is then pressed against the prefabricated FET structure to complete the fabrication. This process allows for the use of any metal or dielectric thin film and any known process of deposition because the substrate for prefabricated structure is silicon. However, a major challenge is the formation of contact between the organic semiconductor and the metal lines. This is particularly important if the structure is to be used for analysing the properties of the semiconductor because contact resistance at the source and drain can significantly reduce device performance. An interesting application of this technique is when there is no gate dielectric deposited, and the airgap between the source/drain terminals from the sides, gate metal from the bottom and organic substrate from the top, is used as the dielectric.

**5.5. Draw the structure of ABS thermoplastic, given that it is an alternating copolymer of the monomers, acrylonitrile ( $C_3H_3N$ ), butadiene ( $C_4H_6$ ), and styrene ( $C_6H_5-C_2H_3$ ).**

**Ans:**



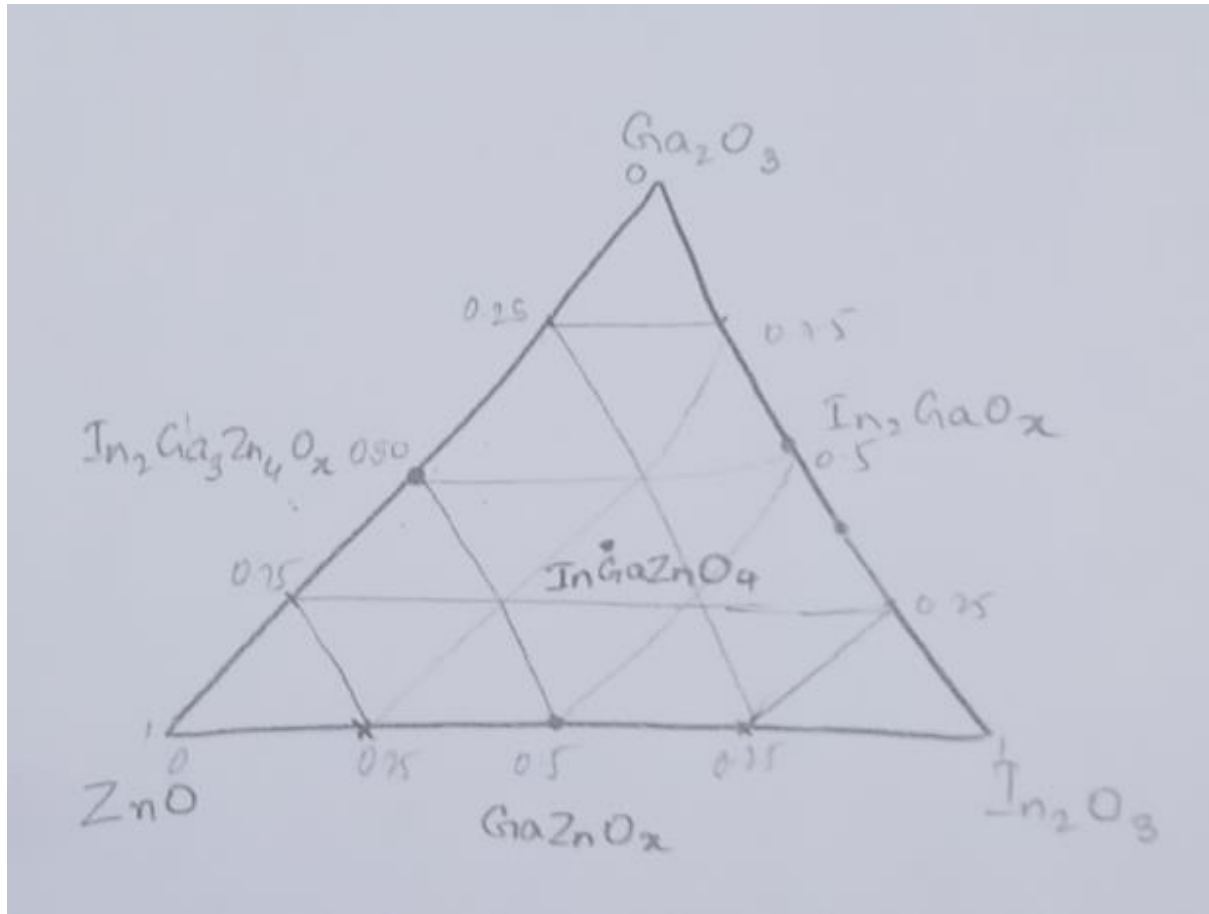


**6.1. What is the fundamental reason for the isotropic conduction of electrons ZnO thins?**

Ans: ZnO is a wide bandgap semiconductor with a direct bandgap of 3.3 eV at room temperature, which makes it a transparent thin film (ideal for display-related applications). ZnO crystallizes in wurtzite structure (named after the naturally occurring ore, ZnS), and can be grown into large, stable, and transparent single crystalline structures. Elemental zinc consists of 30 electrons distributed as  $1s^2 2s^2 2p^6 3s^2 3p^6 4s^2 3d^{10}$  and oxygen has 8 electrons distributed as  $1s^2 2s^2 2p^4$ . In zinc oxide, the electronic states for the conduction band (lowest unoccupied molecular orbital) are determined by the 4s states of zinc, whereas those of the valence band (highest occupied molecular orbital) are determined by the 2p states of oxygen. The involvement of the 4s states of Zn in the formation of the conduction band is significant because s-orbitals are non-directional. Thus, the conduction of electrons in ZnO remains isotropic. Further, in the case of polycrystalline or amorphous thin films of ZnO, the non-directional nature of the 4s orbitals creates a higher probability of overlap with any nearest neighbour molecule, without the consideration of the angle of incidence, leading to a lower occurrence of scattering. Thus, electronic conduction and mobility remain relatively high in polycrystalline or amorphous ZnO compared to conventional semiconductors such as silicon or germanium.

**6.2. Draw the phase diagram for the IGZO system and indicate the following compounds on it:  $\text{InGaZnO}_4$ ,  $\text{ZnO}$ ,  $\text{In}_2\text{GaO}_x$ ,  $\text{In}_2\text{Ga}_3\text{Zn}_4\text{O}_x$ ,  $\text{GaZnO}_x$ .**

**Ans:**



**6.3 Describe the steps for the sol-gel process for deposition of ZnO and zinc tin oxide (ZTO) thin films.**

**Ans:**

ZnO thin films:

The zinc acetate ( $[\text{CH}_3\text{COO}]_2\text{Zn}$ ) is used as the precursor and ethanol as the solvent. The precursor undergoes hydrolysis in the presence of water and alcohol. This is followed by the condensation of two precursor molecules to form a Zn-O-Zn bond, subsequently leading to ZnO particle formation. The solution can then be spin-coated on a substrate followed by annealing at  $300^\circ\text{C}$  for film densification. The sol-gel process can also be used for obtaining ternary and quaternary metal oxide thin films, however, the control of reaction rate of individual metal precursors and obtaining a uniform film composition throughout the film become major challenges. Given the versatility and scalability of the process, some efforts have been made to fabricate thin films of ternary and quaternary metal oxides using the sol-gel process.

ZTO thin films:

Stannic chloride ( $\text{SnCl}_4$ ) is used as the precursor for tin, whereas zinc acetate or zinc chloride ( $\text{ZnCl}_2$ ) can be used as the precursor for zinc. These precursors are separately dissolved, followed by the mixing of the two precursor solutions for the formation of zinc stannate ( $\text{Zn}_2\text{SnO}_4$ ). The sol can then be used to coat a substrate for gel formation, densification, and thin film formation.

**6.4. In the wavy channel architecture, we create fins with 5  $\mu\text{m}$  width, 10  $\mu\text{m}$  depth and with fin pitch of 10  $\mu\text{m}$ . What is the percentage enhancement in the width of the transistor compared to a planar transistor of the same substrate footprint, for a 10 fin structure?**

Ans:

The excess width obtained because of the wavy-channel architecture is the height of the fins. Per fin, the excess width obtained is  $2h$ , where  $h$  is the height of the fin. For a 10-fin structure, this enhancement is  $20h$ . The original width for a 10-fin structure is 100  $\mu\text{m}$ , whereas that with fins is  $100 + 20 \times 10 = 300$ . Hence, there is a 200% increase in the width of the transistor of the same substrate footprint.

**7.1. What is meant by a direct bandgap semiconductor? Why is it important to increase the probability of radiative recombination of carriers?**

**Ans:** When the top of the valence band aligns with the bottom of the conduction band, i.e., when there is no change in the wavevector between these two energy states, then such a bandgap is referred to as a direct bandgap.

In the case of direct bandgap semiconductors, electron excitation and relaxation have a higher probability of occurrence because of electron-photon interactions (low change in wavevector), Thus, in direct bandgap semiconductors, electrons from the excited state have a high probability of radiating a photon to reach the ground state.

**7.2 We decide to create a ternary III-V material from InAs and GaAs that have bandgaps of 0.354 eV and 1.43 eV respectively. If the bowing parameter is 0.436 eV, what is the ratio of InAs required to create a semiconductor that can produce infrared LEDs of wavelength 900 nm?**

**Ans:**  $E_g = xE_{AC} + (1 - x)E_{BC} - bx(1 - x)$

AC=InAs

BC=GaAs

B=0.436 eV

Wavelength = 900 nm=1.378 eV

$$1378 = 354x + (1 - x)1430 - 436x(1 - x)$$

$$\text{Solving we get, } 436x^2 - 2512x + 52 = 0$$

*Solving the quadratic equation, we get  $x = 0.0288$*

**7.3 For the material in question 7.2, what will be the lattice constant if the lattice constants of InAs and GaAs are 0.605 nm and 0.565 nm? If we try to epitaxially deposit the material on a GaAs substrate, what will be the resulting strain in the thin film?**

**Ans:**

$$\text{lattice constant} = xa_{AC} + (1 - x)a_{BC}$$

$$\text{Lattice constant} = 0.0288(0.605) + (1 - 0.0288) * 0.565$$

$$\text{Lattice constant} = 0.56152 \text{ nm}$$

$$\text{Strain } e = \frac{a_{sub} - a_{layer}}{a_{sub}}$$

$$e = \frac{0.565 - 0.566152}{0.565}$$

$$e = -0.0020389$$

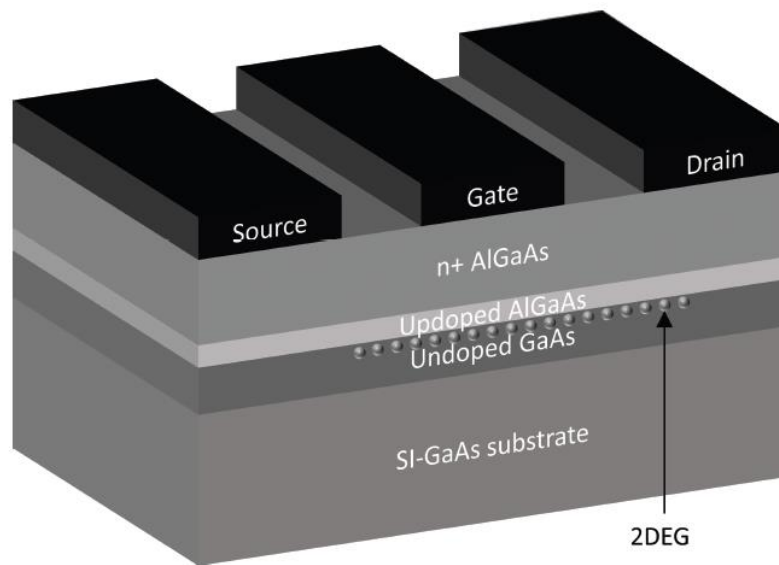
**7.4. Describe the working principle and structure of a high electron mobility transistor (HEMT) based on the GaAs, AlGaAs material system.**

**Ans:** HEMT transistors consist of a junction of two III-V compounds (heterojunction) as the channel, instead of a doped semiconductor. The two materials are chosen such that there is a difference in their bandgap. The material with the wider bandgap is doped to produce excess electrons that migrate to the undoped narrow bandgap material, leading to the formation of a junction. These electrons are then used to transport current through the channel. The accumulated electrons at the edge of the junction are confined to the heterojunction interface, leading to the quantization of energy states. Because these electrons resemble a two-dimensional sheet and are free to move at the junction interface, they are referred to as two-dimensional electron gas (2DEG). In HEMTs, conduction takes place in an undoped material, so the electron mobility obtained is very high, owing to the lack of scattering from dopant atoms.

Working Principle:

The HEMT structure consists of gallium arsenide (GaAs) and aluminium gallium arsenide (AlGaAs). A semi-insulating GaAs substrate is used for the fabrication of the device. A layer of undoped GaAs (bandgap = 1.44 eV) is deposited as the channel material for the formation of 2DEG. This is followed by the deposition of a thin layer of undoped AlGaAs spacer (2–3 nm), followed by n-doped AlGaAs. The undoped spacer is deposited to make sure there is insulation between the 2DEG in the GaAs layer and the doped AlGaAs layer. The gate, source, and drain structures are then created to carry out transistor operations. The electron mobility of III-V materials is very high compared to silicon, leading to very high-speed HEMT devices.





**7.5. What can be the advantages if a trench-protect-etch-release (TPER) process is developed for III-V material systems?**

**Ans:** The process of epitaxy in III-V material systems provides some unique advantages such as:

1. The process is repeatable, a stack of device layers and intermediate sacrificial layers can be grown on the same substrate for producing flexible single-crystal thin films.
2. The process of forming high-quality flexible thin films can be scaled in a way that is not possible for silicon or other material systems. Further, after the process is complete, the wafer can be cleaned, polished, and reused multiple times significantly reducing the fabrication costs.
3. Also, because the thickness of the flexible membranes is determined by epitaxy and their lateral dimensions are determined by photolithography, the overall dimensions of all thin films produced can be repeatable within a certain process window, allowing for reliable industry scale production.

**8.1. Why do electrons behave as if they are massless while travelling through graphene?**

**Ans:** The massless nature of the charge carriers can be predicted from the conical shape of the electronic band at the Dirac point. For other materials, the effective mass of charge carriers is inversely related to the curvature of the energy band with respect to the wavevector. However, in graphene, we have a linear dispersion dependence of energy on momentum, as in the case of photons, with a group velocity of  $1/300$  the speed of light.

**8.2. Describe, in detail, the process for obtaining MoS<sub>2</sub> from elemental molybdenum and sulfur.**

Ans: The process to obtain MoS<sub>2</sub> simply involves the reaction of sulfur vapors with metal thin films at high temperatures. In most cases, sulfur powder and metal thin film deposited on a silicon substrate are introduced in a chamber and heated up to 750°C. The sulfur vaporizes above 444°C and reacts with the metal. This can be used to produce industrial quantities of MS<sub>2</sub> materials on large substrates. The metal thin film can be deposited using physical vapor deposition (PVD) techniques such as evaporation or sputtering. However, the resulting TMD materials with this process are polycrystalline and multilayer, the number of layers depending on the initial thickness of the metal. This can be solved by using a precursor for transition metal instead of the metal thin film such as sulfurization of molybdenum trioxide (MoO<sub>3</sub>) to produce MoS<sub>2</sub>. In this process, MoO<sub>3</sub> and sulfur powders in separate vials are heated in a chamber along with the substrate. This produces thin films of MoS<sub>2</sub> on the substrate.

**8.3. We have fabricated zigzag and armchair CNTs with chiral number  $n = 10$ . What is the diameter of the nanotubes?**

Ans:

Zigzag CNTs:

The zigzag configuration occurs when the vector  $C$  is parallel to the unit vector leading to a situation with the pair  $(n,0)$  which is equal to  $(10,0)$ .

$$\text{Diameter} = |C|/\pi = \frac{\sqrt{((10)^2 + 0)}}{\pi} = 3.18.$$

Armchair CNTs:

The armchair configuration occurs when the vector  $C$  creates an angle of  $30^\circ$ . In this case, the chiral pair is of the form  $(n,n)$  which is equal to  $(10,10)$

$$\text{Diameter} = |C|/\pi = \frac{\sqrt{((10)^2 + (10)^2)}}{\pi} = 4.499.$$

**8.4. What is one of the bottom-up ways of creating metal nanoparticle inks? Give an example for gold NP solution.**

**Ans:** The most commonly used bottom-up process is precipitation. This can be done by creating super-saturated solutions of metal salts by mixing two or more solutions together, or by precipitating metal using a reducing agent. For example, the gold colloids discussed by Michael Faraday in his landmark lecture were created by reducing aqueous chloroauric acid ( $\text{HAuCl}_4$ ) solution.

**8.5. Why does the bandgap of semiconducting nanoparticles (quantum dots) depend on their dimensions?**

**Ans:** The bandgap of semiconducting nanoparticles (quantum dots) depend on their dimensions because of the confinement of the charge carriers. atoms. The boundary conditions at the end of the nanoparticle along with the limited number of nuclei result in an electronic structure that is very different from that of the bulk semiconductor. This results in very interesting electronic and optical properties that are dependent on the shape and size of the QDs. This is a direct consequence of the variation in dispersion of electronic states with the number of atoms present in the lattice.

**9.1. List the ideal properties associated with a substrate for flexible electronics applications. Give two examples of sets of properties that are in conflict with each other, if present in the same material.**

Ans:

1. The substrate material should be flexible. This means the flexural rigidity for a given configuration and flexing axis should be as low as possible. This boils down to having a low Young's modulus for a substrate of given dimensions, or the ability to create ultrathin versions of the substrate, given a material.
2. The substrate material should have a high elastic strain limit to account for large strains in the top and bottom layers associated with the bending motion.
3. The restoring force generated inside the substrate, upon the application of stress, should be high to allow for the substrate to retain its original shape upon removal of stress.
4. Ideal substrates should be able to withstand high temperatures, particularly if the integration strategy involves direct deposition of materials on these substrates.
5. From a usability point of view, ideal substrates should be lightweight and easy to handle independently.
6. Substrates should be easy to manufacture and low-cost to allow for scaling up of device manufacturing.
7. The substrates, particularly in the case of wearable electronics, should be non-toxic and biocompatible.
8. To avoid the build up of stress because of temperature cycling over its lifetime, it is ideal to have a substrate with a low coefficient of thermal expansion (CTE), or with CTE matching that of other materials in the integration.
9. The substrate should ideally have high thermal conductivity so that heat generated because of processing within the flexible electronic device can be dissipated effectively.



10. The substrate should be electrically insulating to make sure different parts of the integrated system are electrically isolated from each other.
11. Ideal substrates should have low water and oxygen permeation to ensure reliable operation of electronics under any deployment condition.
12. An ideal substrate has very low surface roughness, thus, the material and process used for substrate preparation should allow for very smooth surfaces to be fabricated.
13. It is ideal to have a transparent substrate for applications involving optoelectronics such as displays, solar cells, and so on.

It is impossible to obtain a material having all of these ideal properties because many of these properties are conflicting, i.e., having one desirable property implies the loss of another from a basic physics perspective. For example, it is stated that an ideal substrate should be flexible, which requires the Young's modulus of a material to be low, given the dimensions and axis of flexure are fixed. However, low Young's modulus leads to a low spring constant for a substrate of given dimensions, leading to a low restoring force. Thus, there needs to be a balance between the requirement for high restoring force and low flexural rigidity. Similarly, the requirement of high thermal conductivity and electrical insulation results in a very narrow set of materials. Highly crystalline materials such as diamond demonstrate high thermal conductivity due to effective phonon transport through the lattice, while being electrically insulating because of the lack of free carrier concentration at room temperature owing to the tight binding of electrons in the lattice. However, such materials are neither flexible, because the tightly bound lattice leads to a high Young's modulus, nor easy to fabricate, because highly crystalline materials require sophisticated fabrication techniques such as the epitaxial process. Hence, the search for ideal substrates for flexible electronic applications leads to compromises based on the application at hand, functional materials being used, the conditions of deployment, and so on.

**9.2. What are the key advantages/disadvantages of metal foil substrates compared to flexible glass substrates?**

Ans: Metal foil substrates are one of the first substrates to be used for flexible electronics research. Thin steel foils were used to work with organic electronic materials and metal oxide-based thin-film transistors (TFTs) in the 1990s. Steel foils possess many properties listed for an ideal flexible substrate. They are resistant to chemicals, mechanically stable, have high thermal conductance, have low CTE, and can withstand very high temperatures (up to 1000°C). Further, their high electrical conductance can be used to create an easily accessible common ground terminal or for shielding from electromagnetic noise. In particular, the use of steel foil substrates for the fabrication of organic electronic material was popular because of their ability to act as a barrier for oxygen and moisture.

There are several advantages to the use of metal foils as flexible electronic substrates, however, they offer some key disadvantages leading to their reduced popularity. One such problem is the apparent plasticity, or the lack of restoration forces, in a metal foil substrate. We have all experienced the plasticity of metal foils when using aluminium foils to pack food items. This behaviour is unique to metals because of their peculiar bonding structure where electrons are shared among a sea of positively charged kernels. Thus, when displaced due to the application of large strain, metal atoms do not experience restoration forces that covalently or ionically bonded atoms typically face upon being displaced from their equilibrium position. The resulting apparent plasticity can be both detrimental and advantageous for the use of metal foils for flexible electronic applications.

**9.3. Name the key classes of polymers used for flexible substrates, along with the properties of each.**

Ans:

The most commonly used plastic substrates are poly(ethylene terephthalate) (PET) and poly(ethylene naphthalate) (PEN). PET is the polymer of ethylene terephthalate ( $C_{12}H_{14}O_6$ ), which is an ester of ethylene glycol ( $[CH_2OH]_2$ ) and terephthalic acid ( $C_6H_4(COOH)_2$ ), while PEN is a polymer of ethylene naphthalate ( $C_{14}H_{10}O_4$ ), which is an ester of ethylene glycol ( $[CH_2OH]_2$ ) and naphthalenedicarboxylic acid ( $C_{10}H_6(COOH)_2$ ). Both PET and PEN belong to the polyester family. They provide good chemical and mechanical stability. They are highly flexible and can be made transparent for specific wavelength ranges.

Polyimide is another polymer commonly considered as an ideal substrate for many flexible electronic applications. Polyimide is a polymer of the imide monomer, which is a functional group consisting of two acyl moieties attached to a nitrogen atom ( $R_1CO-NR_2-COR_3$ ). Imides are generally formed from dicarboxylic acids through a reaction with ammonia. Polyimides are polymers with the central nitrogen molecule attached to an organic group with another attached to the acyl group ( $[-R_1-CO-NR_2-CO-]_n$ ). Polyimides share some common properties derived from their base structure and composition; however, they can be tuned based on the functional groups  $R_1$  and  $R_2$ . The most important property of polyimides is their relative stability at moderate temperatures compared to other polymer materials.

Silicones are polymers consisting of a siloxane group attached to other organic moieties. The siloxane group consists of an oxygen atom attached to two silicon atoms that are attached to three other groups. Silicones polymers typically include a  $-Si-O-Si-$  chain with the Si atoms being attached to other functional groups ( $[-SiR_1R_2-O-]_n$ ). The simplest of the siloxane polymers is polydimethylsiloxane (PDMS).

**9.4. Describe the transfer printing process, along with the kinds of stamps that can be used for it.**

**Ans:** The process of transferring a set of devices precisely from one location on a substrate to another substrate is referred to as transfer printing. In the simplest example of transfer printing, the host and the destination substrates are pressed together to facilitate the transfer of devices from the former to the latter. In this case, the most important condition for the transfer process to be successful is that the adhesion of the device stack to the host substrate should be lower than that with the destination substrate. This can be made possible using several techniques. The adhesion of a set of thin films on a substrate depends on the surface energy of the substrate, the properties of the thin film, the deposition process, and the post-processing involved. In many cases, devices are detached from the host substrate before the transfer process by etching away some part of the support structure under the device layers. It is common practice to use a “sacrificial” layer to connect the device stack with the host substrate. This layer can then be etched partially or completely to release the devices before being transferred to the destination substrate. The composition of the sacrificial layer and the etch chemistry depends on the device layer and the host substrate. They are chosen such that the etch chemistry has a high etch rate for the sacrificial layer and is also highly selective to the device and the host substrate. Further, in most practical cases, it is not advisable to completely eliminate the sacrificial layer because doing so can release the device layer from the host substrate even before the transfer process. Thus, a small section of the sacrificial layer is preserved to act as a loose connection between the device layer and the host.

Transfer printing is generally done using an intermediate substrate, called a “stamp”, in two steps – pickup and printing. The stamp is a substrate used to host the devices during the transfer process. In the pickup step, the stamp is pressed against the host substrate to transfer the functional devices onto the stamp. In the printing step, the stamp is pressed against the

destination substrate to transfer the devices onto the desired location on the destination substrate. As discussed earlier, it is important that in both steps, the adhesion between the host substrate and devices be lower than that between the devices and the destination substrate. The types of stamp that can be used are:

- a. Viscoelastic Stamp
- b. Thermal Release Stamp
- c. Solvent Release Stamp

**10.1. What is the dominant permeation mechanism for a vapor through a barrier thin film?**

**Ans:** The main mechanism of permeation through a thin film is the diffusion of a permeate from a high concentration region (external world) to a low concentration region (inside the system). This process can take place through the pinhole defects or cracks in the material or a slow process of dissolution or absorption of the gas into the barrier film on one side, movement across the barrier film, and evaporation from the other. Thus, the process of permeation in a medium with no pinholes or cracks involves both solubility of the gas in the material and diffusivity through the material. In case any of these parameters is low, the permeation of a specific gas through the medium is significantly reduced. For example, the diffusivity of a permeate depends on the shape, size, and reactivity of its molecules, and the lattice structure of the barrier material. Thus, dense metallic films have very low material permeability.

**10.2. What are the advantages/disadvantages of ceramic barrier coatings compare to polymer ones? Explain how the use of multiple barrier coatings combining ceramic and polymer will help in creating a better barrier film.**

**Ans:** Metals and ceramics both form dense lattices, but pinholes and defects cause gas ingress into the material through the grain boundaries in amorphous and polycrystalline materials. In the case of ceramics, the brittleness of the underlying material leads to the requirement of much lower thickness resulting in a fragile thin film. Further, the diffusivity through the material increases significantly with the reduction in thickness because the probability of having a through pinhole defect is much higher. Thus, polymer materials are becoming a popular choice for flexible electronics packaging, with low cost and ease of manufacturing. Further, polymer thin films, unlike metal foils, can be transparent, which is essential for use in display and solar cell applications. Most polymer thin films also show highly elastic behaviour for large strains. However, the major disadvantage of the use of polymers for packaging is their high material permeability for moisture and oxygen.

The multiple barrier coatings combining ceramic and polymer will help in creating a better barrier film. The deposition of a thin film of high-density ceramic such as silica or alumina on a polymer substrate should be able to provide a highly impenetrable material that is transparent and easy to handle. However, in practice, this technique can lead to high permeability if pinhole defects and cracks develop on the ceramic thin film in the duration of use, particularly upon repeated flexing. These pinholes lead to the direct contact of the underlying polymer layer with the environment leading to ingress as well as lateral diffusion across the polymer thin film. Thus, multiple small pinholes can be more damaging than a single large defect. To avoid this problem, it is common practice to use multiple alternating layers of ceramic and polymer materials to form a reliable barrier sheet. The use of multiple layers drastically reduces the probability of having a pinhole in all the ceramic layers at the same position.

**10.3. Say we need to have a capacitance per unit area of  $1 \text{ fF}/\mu\text{m}^2$  for our circuits. We have the option of using silicon dioxide ( $\kappa = 4$ ) and aluminum oxide ( $\kappa = 10$ ) as dielectric films. What will be the thicknesses of these films? If the resistivity of the films is the same, what is the change in leakage current going from  $\text{SiO}_2$  to  $\text{Al}_2\text{O}_3$  dielectric?**

**Ans:**  $C_{ox} = 1 \text{ fF}/\mu\text{m}^2$

$$C_{ox} = \frac{k\epsilon_0}{t}$$

$$t = \frac{k\epsilon_0}{C_{ox}}$$

For  $k = 4$ ,  $t = 35.2 \text{ nm}$

For  $k = 10$ ,  $t = 88 \text{ nm}$

The leakage current depends on the resistance offered by the films, which is dependent on their thickness. Higher thickness leads to higher resistance, and thus less leakage current for  $\text{Al}_2\text{O}_3$  compared to  $\text{SiO}_2$ .



**10.4. We are planning to select a barrier thin film for flexible electronic applications. Suppose the requirement maximum vapor transmission rate is given as 1 mg/m<sup>2</sup>-day. The maximum absolute humidity of the deployment location is going to be 30 g/m<sup>3</sup>. If we are constrained to use a film of thickness 10 μm, what should be the diffusion coefficient of water vapor through it?**

Ans:

$$J = D \frac{dC}{dx}$$

$$J = 1 \text{ mg/m}^2\text{-day}$$

$$dC (\text{max}) = 30 \text{ g/m}^3$$

$$dx = 10 \text{ μm}$$

Thus,

$$D = \frac{J}{\frac{dC}{dx}} = \frac{0.001}{\frac{30}{10^{-5}}} = 3.33 * 10^{-2} \text{ cm}^4/\text{day}$$

**10.5. What are some of the organic alternatives for high- $\kappa$  dielectric thin films for flexible electronic devices?**

**Ans:** Polyimide (PI), polymethyl methacrylate (PMMA), polystyrene (PS), and SU-8 are some of the organic alternatives.

One of the polyimides commercially available in liquid form is the PI-26xx series from HD Micro Systems.

Polyvinylidene fluoride (PDVF) is commonly used in the electronics industry as wire wrap, known for its stability and insulating properties. It is a polymer of vinylidene fluoride or 1,1-difluoroethene ( $\text{CH}_2\text{CF}_2$ ).

**11.1. What are the considerations for materials for the substrate and metal layers of flexible PCBs? Which materials are commonly used for substrate and metal layer?**

Ans: The base material of a PCB should be electrically insulating and mechanically stable, and still have reasonable flexibility required by the application. The material should also be compatible with the metal layer, adhesive layer, cover layer materials, and the materials used for fabrication processes such as patterning, etching, dicing, and so on. The typical substrates used for fPCB manufacturing include polyimide, polyether ether ketone (PEEK), or polyester (Mylar, PET, PEN) thin films. The most commonly used substrate material is polyimide because of its electrical, thermal, chemical, and mechanical stability. Polyimide thin films cost significantly more than polyesters, however, their thermal and chemical stability compared to polyester thin films gives them a distinct advantage as a base for fPCBs. Thermal stability is of prime importance for PCB manufacturing because the soldering of components is performed at elevated temperatures. Polyesters are used if the integration has specific design requirements, for example, if transparency is required as part of the system design.

**11.2. What are flexible hybrid electronic systems? What are their advantages and disadvantages?**

**Ans:** The use of fPCBs with rigid, conventional components leads to “semi-flexible” or Flexible Hybrid Electronic (FHE) systems.

Advantages:

1. It provides an opportunity to use devices based on state-of-the-art, scaled silicon CMOS technology. Further, the fabrication and patterning of fPCBs are done using well-established and scalable processes. This leads to high-performance electronic systems that have the ability to reversibly bend, flex and twist.
2. The use of fPCBs is the lower weight and thickness of the overall assembly compared to that obtained with conventional PCBs. This is of great significance for modern applications with wearable and healthcare monitoring systems becoming the norm. The use of fPCBs in these systems allows more components to be packed into the same thickness, resulting in higher performance and functionality.
3. The lower thickness also allows for the heat generated in the circuit components to flow out more efficiently, resulting in better thermal performance of the overall system.

Disadvantages:

1. Cost: The use of flexible layers increases the manufacturing complexity of the process. For example, the use of roll-to-roll processing requires that the tension in the entire web, sometimes a few feet in width, be uniform throughout the process. This requires high-end manufacturing tools leading to an increase in costs.
2. In some designs, the holes in the cover layer need to be overlaid on the conductive pads with an alignment error window of a few microns. Such an alignment accuracy is difficult to obtain and maintain throughout the R2R process.

**11.3. What are the advantages of rigid-flex integration? Provide an example of a commercial product employing rigid-flex assembly.**

**Ans:** An integration strategy that combines the fPCB and conventional rigid PCB in the same system resulting in a final PCB that includes parts assembled on a fPCB and those on a rigid PCB connected together in a “Rigid-Flex” PCB. In the case of a combined integration strategy for fabrication, the process typically starts with a single layer of the flexible or rigid part. The process for overlay covering, drilling and plating is followed in a similar way as for individual rigid or fPCB fabrication. The difference is that the rigid and flexible layers are already patterned into the final design structure and combined into a single PCB structure at the final stages of processing. This strategy allows the designers to optimize the PCB area, given that there is no need for separate connection ports on either the flexible or rigid parts. The tail end of the process, which includes surface finishing, milling, forming, etc., is undertaken by the rigid-flex assembly as a single unit leading to seamless and more reliable interconnections.

The benefits of rigid-flex integration have resulted in the use of this strategy for many commercial applications, not only related to flexible or wearable electronic systems. We find rigid-flex PCBs in the dashboards of automobiles, inside computers, printers, laptops, and most of the electronic systems around us. The flexible part is mostly used for interconnection, thus, having no electronic components attached to it.

**11.4. Why can we not use small silicon chips integrated on flexible PCBs to create a fully flexible system?**

**Ans:** The key problem with the use of small chips is that the power dissipated in the system is concentrated at these points. Compared to an integration with large area chips with built-in heat sink and thermal management, a system based on small discrete chips may result in much higher power density and temperature for the same power dissipation. Such a system will then require much better thermal design and implementation, adding to the total cost. However, this approach does provide a way to obtain flexible, high-performance electronic systems with state-of-the-art silicon components and well-established fabrication processes.

**12.1. Describe the advantages/disadvantages of CIJ and DoD methods for inkjet printing.**

**Ans:** In the CIJ method, there is a continuous stream of droplets emerging from the nozzle. The substrate is attached to a movable stage to control the design formed and its location on the substrate. In some designs, there is a provision to stop the stream of droplets from reaching the substrate. In the case of DoD, the droplets are only formed when the deposition is required on the substrate. In both cases, the actuation can be provided by creating a pressure wave inside the chamber using a piezoelectric membrane, thermal expansion, or acoustic actuation.

The key difference between CIJ and DoD, i.e., the ability to switch the droplet stream on/off, provides for the advantages and disadvantages of the technologies. With CIJ, because the droplet stream is continuous, there is consistency in the size of droplets obtained, leading to a simpler design of the actuation mechanism and nozzle. Further, there is no danger of the ink drying out and clogging the nozzle head, which is ever-present in the DoD method. On the other hand, the DoD method provides more freedom and precision in the design to be printed, without the wasteful diversion of the ink stream. For this reason, most of the laboratory setups employ the DoD methodology, while industrial ones use CIJ. DoD is particularly important in the case of printing systems involving multiple heads and materials because the duty cycle of each nozzle is very low. Hence, it is not ideal to have a continuous stream of droplets from all the nozzles at all times. However, prolonged inactivity of a nozzle head can lead to changes in the fluid at the opening of the nozzle, which may result in sedimentation or clogging.

**12.2. We plan to create an ink based on water as the solvent. What is the nozzle diameter required to obtain an Ohnesorge number of 0.2 at 30 °C? (consider the properties of pure water).**

**Ans:**

$$Oh = \frac{\mu}{\sqrt{\rho \sigma d}}$$

$$d = \frac{\mu^2}{\rho \sigma Oh^2}$$

Using the values of surface tension, density and viscosity for water at 30 °C,  $d = 0.3 \mu m$ .

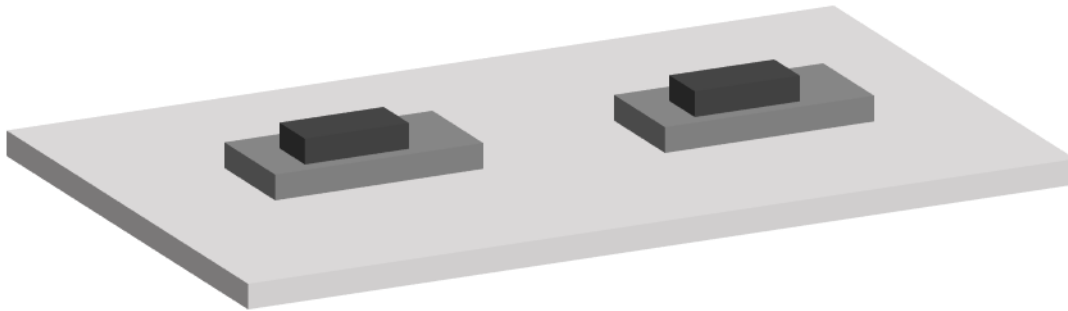


**12.3. Describe the screen printing and flexographic printing techniques for obtaining patterns on flexible substrates in detail.**

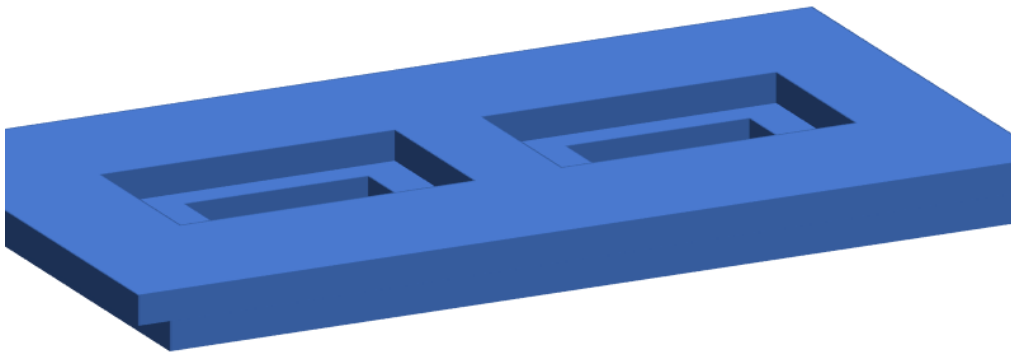
**Ans:** In screen printing, a porous mesh screen containing the ink is pressed against the substrate to transfer the ink onto the substrate. There is a stencil or mask separating the substrate and the screen for determining the pattern of the ink. The ink is typically applied to the screen using a blading process, while the reverse stroke is used to press the screen against the substrate to obtain the pattern. In particular, it is important to have a higher viscosity ink to facilitate its application on the screen. Further, the transfusion through the screen requires the particle size to be strictly regulated, and very little coagulation of nanoparticles can be allowed before application on the screen. The key advantage of this process is the speed at which a large area of the substrate can be printed, greatly increasing the process throughput compared to inkjet printing. The disadvantage of this process is the use of a physical mask which does not allow for dynamic variation in the pattern design, as in the case of inkjet printing. Further, the process involves the physical contact of the screen and the substrate, which may not be appropriate for delicate or uneven substrates.

Flexographic printing is based on the R2R process used for printing on paper, for example, in the printing of currency notes. The process involves the use of a printing plate with pattern structures raised from the surface, similar to a rubber stamp. The printing plate is attached to a roller that gets wetted in the ink from an ink bath and deposits the ink onto the substrate through physical contact. The pattern is obtained because the substrate only makes contact with the raised structures on the printing plate. This process is an extremely high throughput process, capable of printing a large area substrate (large width), and is perfectly suited for R2R manufacturing process (Figure 12.6). However, the key disadvantages are the high setup cost involved, particularly for the manufacturing of the printing plate with high-resolution structures.

**12.4. Given the pattern in the figure below, design a mold that can be used to achieve it using the SAIL process.**



**Ans:**



**12.5. Enumerate the advantages and disadvantages of the nanoimprint lithography (NIL) process.**

**Ans:**

**Advantages:**

The most important advantage of the NIL process is the ability to create high resolution patterns using a simple process. Line resolution of a few tens of nanometers is easily achievable using NIL, which would conventionally require high-end photolithography equipment that accounts for a significant portion of the cost of CMOS manufacturing because of the use of precision control systems and optical lenses to obtain nanometer-scale resolution. Additionally, the photoresists used in the conventional lithography systems are precisely engineered to obtain a certain thickness and optical sensitivity at a particular wavelength, whereas, the simplicity of the NIL process permits the use of any polymer or composite with tunable fluidity as the resist material. Further, the NIL process can be used to transfer large-area patterns onto thin films in a single step. The process thus provides the ability to create high-resolution patterns at a much faster pace compared to photolithography. The process is also compatible with flexible substrates and with the R2R manufacturing technique.

**Disadvantages:**

One of the major problems in NIL is the accuracy of aligning the mold pattern with patterns already present on the substrate, referred to as overlay accuracy. The overlay accuracy in conventional lithography is obtained using mask registration by moving the mask or wafer stage to obtain alignment before exposure is carried out. This process is tricky with a mold because of the need for transparent (or through etched) registration windows. Further, the topological patterns on the mold would require higher clearance from the wafer leading to less

accurate registration. Another problem with the use of molds for pattern transfer is damage and wear over successive uses.

**13.1. Explain the effect of dimensional scaling of CMOS transistors, and the voltage, on the drive current, speed, and power dissipation.**

**Ans:** The success of silicon CMOS has been because of the dimensional scaling of transistors. Let us consider that we change the linear dimensions of all the components in the chip by a constant scaling factor “ $s$ ” ( $>1$ ), This leads to a reduction in the width and length of the transistor, and thickness of the dielectric by the same scaling factor, whereas material properties like mobility are unaffected. The capacitance per unit area increases proportionally because of the decrease in dielectric thickness, leading to a proportional increase in the drain current, because the  $(W/L)$  ratio remains constant. The gate capacitance decreases because the area reduction is more than the gain from the reduction in dielectric thickness. This reduction in gate capacitance along with an increase in drain current leads to a much better switching time. These changes bode well for the speed of the processor. However, the problem is with the power dissipation, which increases proportionally to  $s$ . This power is for a single transistor and is now dissipated in a smaller area, leading to a much higher power density. The explosion in power density with scaling would have acted as a major problem in the argument for dimensional scaling. However, the way this situation is mitigated is by scaling the voltage proportionally as well. These changes, applied along with the dimensional scaling, cause the drain current to reduce by a factor of  $s$ , however, this does not cause a slowing down of the processor because of the reduction in drain voltage. Thus, switching time still reduces by a factor of  $s$ . Further, because of the reduction in voltage and current, the power dissipation reduces by a factor of  $s^2$ , while the power density remains the same. Thus, higher switching speed and better device density are obtained even with the same power dissipation density. This win-win situation is the reason for the success of dimensional scaling of silicon processors. Dimensional scaling of the semiconductor manufacturing process is designated by the size of the minimum feature of the chip.

**13.2. Assume we fabricated a transistor with a semiconductor with mobility of 1000 cm<sup>2</sup>/V-s, the dielectric thickness of 2 nm, κ-value of 10, V<sub>dd</sub> of 3 V, V<sub>t</sub> of 1 V, and W=L=100 nm. What is the saturation drive current expected from the transistor? If this transistor is used to drive the gate of another such transistor, how much time is needed to charge it to V<sub>dd</sub>? What is the power dissipated during switching?**

**Ans:** Mobility= 1000 cm<sup>2</sup>/V-s

dielectric thickness = 2 nm

κ=10

V<sub>dd</sub> = 3 V

V<sub>t</sub> = 1 V

W=L=100 nm.

$$I_d = \frac{\mu_n C_{ox} W}{L} (V_{dd} - V_t)^2$$

$$I_d = 1000 * 0.01^2 * 10 * 8.854 * \frac{10^{-12}(3 - 1)}{2 * 10^{-9}}$$

$$I_d = 8.854 \text{ mA}$$

$$C_{ox} = 44.25 * 10^{-3} \text{ F}$$

$$C_g = C_{ox} * A$$

$$C_g = 44.25 * 10^{-3} * 10^{-14} \text{ F}$$

$$C_g = 44.25 * 10^{-17} \text{ F}$$

$$Time = \frac{C_g V_{dd}}{I_d}$$

$$Time = 44.25 * 10^{-17} * \frac{3}{8.854 \text{ m}}$$

$$Time = 0.15 * 10^{-12} \text{ s}$$

$$Power = \frac{CV^2}{T}$$

$$Power = 26.55 \text{ mW}$$

**13.3. If the transistor of question 13.2 is scaled by a factor of 2, what are the new values of drive current, charging time, and power dissipation?**

**Ans:**

$$I_{d1} = \frac{I_d}{s}$$

$$I_{d1} = 4.427 \text{ mA}$$

$$T_1 = \frac{T}{s}$$

$$T_1 = 0.075 * 10^{-12}$$

$$P_1 = \frac{P}{s^2}$$

$$P_1 = 13.275 \text{ mW}$$

**13.4. What are the key properties that a material system needs to possess to obtain large-area CMOS circuits? Compare the following material systems on these properties: silicon, organic semiconductors, metal oxide semiconductors, nanostructured material systems.**

**Ans:** Material selection and process flow are key to the performance of the transistor. Further, these parameters also determine the speed of the gates formed using the transistor (switching speed), thus determining the speed of the entire processor. The last piece of the processor puzzle is the number of transistors (and hence gates) per unit area of the chip, also known as the device density. This parameter determines the complexity and sophistication of the processor architecture. A higher device density leads to more gates per unit area, allowing for more complex architecture, leading to a processor with more functionality. Thus, semiconductor material and process flow are two independent variables that determine the drain current, switching speed, power dissipation, and device density. These parameters, in turn, determine the performance of the processor. However, it should be noted that these parameters are not independent of each other. For example, changing the dimensions of the transistor to increase device density, also changes its current characteristics and switching speed.

The success of large-scale flexible circuits made using non-silicon semiconductors depends on the ability of these materials to form dimensionally scaled CMOS devices. Presently, research is going on, on potential replacements for silicon – metal oxides, organics, TMDs, and so on. However, there remain key challenges in the integration of these materials into largescale CMOS circuits that could challenge the supremacy of silicon. At present, it seems device-first flexible silicon processes are the most promising for obtaining state-of-the-art processor capability in a flexible form. However, non-silicon semiconductors have already found mainstream commercial success in other areas of electronic system design such as memory,



displays, photovoltaics, energy storage, and so on. These use cases do not require large-scale CMOS integration, dimensional scaling, or precise threshold voltage control.

**13.5. Describe the phenomenon of ohmic contact between a metal and semiconductor for n-type and p-type materials.**

**Ans:** Ohmic contacts are junctions between two disparate conductive mediums such that there can be non-rectifying charge transfer in both directions, i.e., the current-voltage characteristic of the junction is linear. Whether a metal will form such an ohmic contact with a semiconductor depends on the Fermi energy levels of the metal and the semiconductor (their work functions). In the case of n-type semiconductors, the work function of the metal should be less than that of the semiconductor to form Ohmic contacts, whereas, in a p-type semiconductor, the work function of the metal should be more.

**14.1. Explain the different levels of memory hierarchy. Why are they typically represented as a pyramid?**

**Ans:**

Within volatile memories, there are some memory blocks that are positioned very close to the processor for immediate access and information caching, called level 0 (L0). These are generally formed using arrays of registers. These blocks obtain information from level 1 storage, called L1 cache, which is typically made using SRAM cells and is located on the same chip as the processing units. It has a larger storage space, compared to L0 cache, to provide for more information to be buffered for the processor to fetch from. The main memory, also called primary memory, or RAM of the system is the level 2 storage that typically exists as a separate memory chip. Finally, the disk storage, or the non-volatile memory, is the level 3 storage that provides permanent information such as coded instructions, files, data, and so on. These levels typically form a pyramid, because the storage available increases as one goes from level 0 to level 3. For example, a processor contains a register bank of a few hundred bytes at level 0, and a volatile memory of hundreds of kilobytes to few megabytes at level 1. The main memory (at level 2) these days consists of a few gigabytes, whereas the non-volatile disk storage (at level 3) is typically a few terabytes. The levels of memory are typically depicted as a pyramid because the storage size increases going from level 0 to level 3. The memory units are lower levels are smaller, closer to the processor core, and faster.

**14.2. What are the key challenges in creating flexible volatile memory modules? Give examples of a few methods that can be used to create flexible volatile memories.**

**Ans:** While the individual cell is a relatively simple construction in both SRAM and DRAM, the complexity of the read/write circuit creates a problem while creating flexible versions of volatile memory. In particular, the read operation in both SRAM and DRAM cells requires the use of high precision sense amplifiers, which can be difficult to integrate on a flexible platform. Hence, reports in the literature pertaining to demonstrations of random-access memories only focus on the implementation of the cell, particularly as a technology demonstration for a novel thin film or integration process, without implementing the interface circuits. For example, an SRAM cell was fabricated using Dinaphthothienothiophene (DNTT, C<sub>22</sub>S<sub>2</sub>H<sub>12</sub>) as the semiconductor. This and other such demonstrations have been important first steps, following which larger arrays of SRAMs were fabricated on flexible substrates. In the few cases when large arrays or interface circuits have been demonstrated along with the memory cell array, the integration has been performed using thin-film transistors (TFTs) based on large-area uniform thin films such as metal oxides, polymers, and polysilicon. In these integrations, the thin film is typically deposited on a flexible substrate using a low-temperature process such as sputtering. The memory cell and the interface circuitry are then fabricated using standard lithography processes. For example, a flexible 16 kb memory was demonstrated using TFTs based on low-temperature polysilicon as the semiconductor. The devices were fabricated on a glass substrate and transferred onto a 0.2-mm thick flexible plastic substrate. This system, consisting of 110,000 transistors, included the interface circuit on the flexible platform. Another such example is the demonstration of a 128-bit SRAM array (16x8), along with the interface circuit, fabricated using amorphous indium gallium zinc oxide (a-IGZO) as the semiconductor on a flexible polyimide substrate.

**14.3. Describe, in brief, the working principle of the following non-volatile memories:**

- **Resistive RAM**
- **Phase change RAM**
- **Floating gate flash memory**

**Ans:**

Resistive RAM:

In resistive RAMs, or memristors, the resistance of an oxide thin film is changed by causing a soft breakdown by applying a set voltage. The application of reset voltage reverses the condition of the thin film. A high resistance oxide is read as logic 0, while a low resistance is read as logic 1.

Phase change RAM:

In phase change RAM, the phase of a thin film is changed from amorphous to crystalline and back by applying pulses of current, or through optical excitation.

Floating gate flash memory:

Flash memory has the same structure as that of a MOSFET, with the difference that there is an additional isolated thin film in the gate stack acting as the floating gate (FG). This conductive thin film is isolated from the channel using a tunnelling oxide layer and from the gate metal using a blocking oxide layer. The threshold voltage of the transistor depends on the number of charges trapped inside the FG layer. Information stored in the transistor is changed by causing charges to tunnel into the conductive layer through the semiconductor channel and change the threshold voltage of the underlying transistor. Flash memory is the most commonly used NVM technology for manufacturing solid-state drives, memory cards, USB drives, and so on.

**14.4. Describe how an organic polymer material, PVDF TrFE, behaves as a ferroelectric thin film. How can this property be used for fabricating a non-volatile memory? What are the challenges associated with it?**

**Ans:**

An organic material known as PVDF-TrFE is commonly used as a ferroelectric thin film for FeRAM applications. PVDF-TrFE, or poly(vinylidene fluoride-trifluoroethylene), is a copolymer consisting of vinylidene fluoride (VDF) and trifluoroethylene (TrFE) monomers. The copolymer contains randomly oriented dipoles because of the presence of a heavily electronegative fluorine atom. An example of a flexible FeRAM based on PVDF-TrFE as the ferroelectric thin film. The structure was based on a transistor configuration (1T), wherein the ferroelectric material thin film is used as an addition to the gate stack. The transistor was fabricated on a flexible PEN substrate using ALD-deposited ZnO thin film as the semiconductor and Ti/Au/Ti as the source/drain contact metal. In such a structure, information is stored in the form of polarization of the ferroelectric gate insulator layer, which changes the turn-on voltage of the underlying transistor. This change in  $V_{on}$  can be used to sense the stored information. The wordline is typically connected to the gate, whereas the source and drain are connected to bitline and ground. When wordline is activated, the current in the bitline depends on the polarization of the ferroelectric layer, which is sensed to determine its state. For the write operation, the polarization is set by applying a specific electric field across the gate and the channel.

**14.5. Why haven't several flexible versions of flash memory been reported in the literature, even though the rigid versions are the most mature NVM technology?**

**Ans:** The integration strategy used for flexible volatile memories, owing to their proximity to the processor, is dependent on the integration strategy used for fabricating the process. The increased use of NVM SSD technologies in electronic devices has increased emphasis on research in rigid NVM technologies, leading to progress in their flexible forms as well. The progress is particularly clear in the various rigid flash memory architectures, however, progress in flexible flash memory has been slow. The crossbar architectures afforded by ReRAM, FeRAM, and PCRAM provide a facile strategy for fabricating flexible versions of their memory cells. However, for the memory module to be complete, the interface circuit should also be flexible, requiring flexible CMOS transistors, gates, amplifiers, and flip-flops to be fabricated. Thus, the progress of flexible memory modules is eventually tied with the overall progress in flexible electronics fabrication.

**15.1. Describe the working principle of the liquid crystal display (LCD). What are the challenges in fabricating a flexible LCD?**

Ans: The LCD technology, uses the light polarizing property of liquid crystals. LCD pixels act as a gateway for light, inhibiting or allowing light to pass through depending on the applied electric field. LCD pixels cannot produce light but can only modulate the passage of light. Thus, LCD screens depend on another light emission technology as the source of light, generally acting as the backlight panel. An LCD panel is composed of three basic layers: two glass sheets with polarization orthogonal to each other, sandwiching a layer of liquid crystals. The glass sheets also need to have transparent conductors for the passage of electric current through to the liquid crystal pixels. Further, the glass sheets are coated with a polymer with grooves aligned to the direction of polarization. Thus, in steady state, the liquid crystal molecules gradually twist from one orientation to another. The operation of LCD pixels depends on the fact that liquid crystal molecules can polarize light passing through in a particular direction. The light from the back panel enters the first glass sheet and gets polarized in a particular direction. The direction of polarization of light is then gradually changed as light passes through the liquid crystal. When light exits the liquid crystal film, its polarization is aligned with that of the second glass sheet, allowing it to pass through. However, if an electric field is applied, the orientation of the molecules inside the liquid crystal gets disturbed. This causes the light exiting the liquid crystal to be of a different orientation than that of the second glass sheet, thus, no light passes through the pixel. This control of whether light is allowed to pass, at an individual pixel level, allows for the creation of LCD displays. The source of light can be a CFL (compact fluorescent lamp) or LED panel.

**Challenges:**

There are several challenges in creating flexible versions of LCD displays. The display is based on a backlight obstruction mechanism, it can be challenging to create LCD pixel with a small



bending radius, because the light entering from the back panel may get misaligned with the front end polarized layer, leading to dead pixels. Further, the liquid crystal layer depends on the movement of molecules to create the change in polarization required for the pixel to work. Flexing such a structure can cause issues with the reliability of the movement and light polarization.

**15.2. How is the emergence of quantum dot (QD) technology helping create better displays?**

Ans: The semiconductor quantum dots (QDs) (zero-dimensional nanostructured materials) have been introduced as the functional constituents of the filter layer. As the dimensions of a semiconductor particle approach nanometer scale ( $<100$  nm), its bandgap can be tuned by changing its dimensions. This property arises from the confinement of charge carriers leading to a higher dispersion in the available energy states. Thus, the emission wavelength of a QD can be finely tuned merely by changing its dimensions. The QDs, used for creating the color filtering thin films in LCD displays, are sized such that they produce almost purely monochromatic red, green, and blue colors of a specific wavelength. These particles absorb the incoming blue light from the back panel and emit the specific wavelength they are tuned for. Thus, the LCD displays based on QD thin-film color filters provide better color gamut coverage and perfect black levels.

**15.3. Why are organic semiconductors better suited for fabricating flexible displays compared to inorganic ones?**

Ans: Organic materials have been known to have electroluminescence for decades, however, practical organic LEDs have only been made in the 1990s. The basic working principle of OLEDs is the same as that of LEDs based on III-V materials, i.e., a semiconductor with a certain bandgap is injected with excess charge carriers, which recombine radiatively to create photons. The intensity of the light emitted is proportional to the current (amount of charge carriers injected) and the wavelength is dependent on the energy bandgap of the semiconductor. In the case of organic semiconductors, the energy bandgap is the difference in energy of the highest occupied and lowest unoccupied molecular orbitals (HOMO and LUMO). Charge injection into the semiconductor is done through metal contacts that form Ohmic contacts with the semiconductor, which requires their Fermi levels to be close. However, because the Fermi energy of organic semiconductors cannot be tuned as easily as III-V semiconductors (say through doping), the injection of charges into light-emitting organic semiconductors can be challenging.

**15.4. What is the key difference between passive matrix and active matrix configurations?**

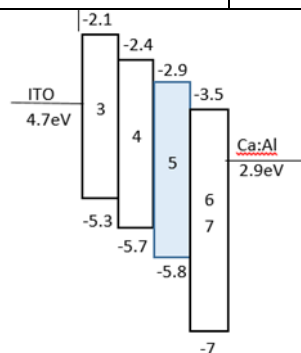
**Why are active matrix displays more popular than passive matrix?**

**Ans:** For both LCD and LED displays, the two main strategies used for pixel control are the passive matrix and the active-matrix strategies. In the passive matrix strategy, the pixels are addressed directly using control lines corresponding to the particular row and column, without the use of a switch. The electronic structure is similar to the crossbar architecture discussed for memory applications. When an electric potential is applied between a particular row and column line, the pixel in the corresponding row and column is activated. This strategy provides for simple fabrication because of the absence of an electronic select switch. However, the lack of the switch also creates problems like crosstalk and sneak path current issues. The problem is typically solved using the active-matrix strategy involving an electronic select switch (typically a thin-film transistor) for controlling each pixel. The presence of the switch resolves the crosstalk problem resulting in better optical contrast; however, it requires the integration of an additional component in the pixel, leading to a more complex and expensive fabrication process. The advantages of the active matrix strategy outweigh these problems, leading to their widespread adoption in the commercial display industry, including television screens, computers, laptops, and mobile phones.

**15.5. We need to design a flexible OLED stack for the visible region. We have the following materials: (a) ITO [WF: 4.7 eV]; (b) Ca:Al [WF: 2.9 eV]; (c) Tris(4-carbazoyl-9-ylphenyl)amine (TCTA) [IP: 5.7 eV, EA: 2.4 eV]; (d) 2,9-dimethyl-4,7-diphenyl-1,10-phenanthroline (BCP) [IP: 7 eV, EA: 3.5 eV]; (e) CuI [IP: 5.3 eV, EA: 2.1 eV]; (f) 4,4'-(9H,9'H-[3,3'-bicarbazole]-9,9'-diyl)bis(3-(trifluoromethyl)benzonitrile) (pCNBCzoCF3) [IP: 5.8 eV, EA: 2.9 eV]. Which of these should be used as the anode, cathode, hole injection, hole transport, emission, hole blocking and electron transmission layers. Explain your choices. What will be the color of the LED?**

**Ans:**

1	Anode	ITO
2	Cathode	Ca:Al
3	Hole Injection	CuI
4	Hole transport	TCTA
5	Emission	pCNBCzoCF3
6	Hole Blocking	BCP
7	Electron transmission	BCP



1. Anode: ITO is selected as anode as it has a larger work function creating a large electron injection barrier.
2. Cathode: Ca:Al is selected as cathode as it has a small work function.
3. Hole Injection: CuI is used as a hole injection layer as it has a lower IP.
4. Hole transport: TCTA is used as hole transport material as it has a lower IP.

5. Emission: pCNBCzoCF<sub>3</sub> is used as an emitting layer as it has an appropriate IE and EA and can accept both holes and electrons
  6. Hole Blocking: BCP is used as a hole blocking layer as it has a larger IP.
  7. Electron Transmission: BCP is used as an Electron transmitting material as it has good electron affinity to accept the electrons
- The color of the OLED will be sky blue.

**16.1. We plan to deploy a solar cell for power a system that requires a constant power of 2 W. The average daily solar irradiation is 1000 Wh/m<sup>2</sup>. What should be the area of the solar cell if the module efficiency is 20%? What should be the capacity of the battery connected to this solar cell so that constant circuit operation is ensured? What will be the area and battery capacity if the solar cell efficiency is 10%?**

**Ans:**

Total energy required for the circuit, per day =  $2 \times 24 = 48$  Wh

When Efficiency = 20%

Total energy output = Total Area x Solar Irradiance x Conversion Efficiency

$$Total\ area = \frac{48}{1000 * 0.20} = 0.24\ m^2$$

Assuming the battery should be able to last for half a day (during the night), we should have a battery capacity of 24 Wh, at the least. To account for gloomy days, a battery of 48 Wh can be used.

When Efficiency = 10%

$$Total\ area = \frac{48}{1000 * 0.10} = 0.48\ m^2$$

The battery considerations do not change with solar cell efficiency.

**16.2. Why is the bonding energy of an exciton higher in organic materials compared to inorganic? What effect does this have on organic photovoltaic cell design?**

**Ans:** In organic semiconductors the binding energy associated with these excitons is much more than that in inorganic semiconductors. This is because inorganic lattice semiconductors typically have a higher dielectric constant compared to organic semiconductors, which leads to a reduction in the Coulomb attraction between excited electron-hole pairs due to dielectric screening. The binding energy of the exciton is a few tens of meV in inorganic semiconductors, whereas it is of the order of hundreds of meV in organic semiconductors. Thus, the excitons created in organic semiconductors are harder to dissociate into individual free charge carriers. If they do not dissociate in time, excitons typically recombine and give out the stored energy in the form of radiation or heat. This can be great for fabricating LEDs, because there is a greater probability for electron-hole recombination and photon emission, however, for photovoltaics, this is a cause of concern, because the conversion of a photon into electric current requires dissociation of the electron-hole pair. This problem is solved in OPVs using the layered structure of organic thin-film semiconductors. The absorption layer is divided into electron donor (ED) and electron acceptor (EA) layers such that the difference between their HUMO and LOMO energy levels is more than the binding energy of the exciton. This promotes spontaneous dissociation of the exciton into electron and hole – the electron is captured by the EA layer while the hole is captured by the ED layer. These charge carriers are then collected by the metal contacts for conduction in the external circuit. This structure is similar to the p-n junction in a silicon solar cell, however, there is no built-in potential or depletion at the OPV layer junction, which implies that there is no force making the carriers drift toward the junction. The excitons created in the OPV cell can only diffuse randomly toward the junction and get separated into individual charge carriers.



**16.3. What are the major energy harvesting technologies involving thin film fabrication technology? What are their relative advantages/disadvantages?**

**Ans:** The rise of wearable and IoT devices has created a use-case for technologies harvesting usable electrical energy from no particular source, i.e., from ambient energy. These include the use of piezoelectric generators to capture energy from movement, triboelectric generators to capture energy from stray charges, and thermoelectric generators to capture energy from temperature differences. These energy sources are already present in the ambient environment of the user. Because the use-case for these energy harvesters typically exists in the wearable, IoT, and biomedical fields, there has been significant effort in making flexible versions of these devices. The structure of triboelectric generators involves the use of two thin films touching each other. These films can be either inorganic or organic polymer materials and are typically held together only at the edges, without the use of an interlayer binding material. Metal electrode thin films are deposited on either side of the bilayer to connect the device to the external circuit. When the two active layers touch or rub against each other, opposite charges accumulate on their surface. This leads to an electric field being generated that induces opposite charges on the metal electrodes. The change in the capacitance of the system, because of bending, causes a current to flow in the external circuit, performing electrical work. When the system is released, a reverse current is induced in the external circuit. Thus, the electrical current generated by the system resembles an alternating current generation system for periodic bending cycles. The key advantage of the use of triboelectric generators is the simple design of the system. Commonly available low-cost organic polymer materials such as polyimide (Kapton), polytetrafluoroethylene (PTFE), PDMS, PMMA, PET, etc., have been shown to be promising active material layers for the fabrication of triboelectric generators. Triboelectricity also has the potential to produce very high voltages, of the order of hundreds of volts open-circuit voltage (Voc). Further, because the system is based on thin films attached together, it

can be made to be completely flexible, providing an opportunity for attaching to any surface for harvesting energy.

The major disadvantage is that the amount of power generated per cycle of motion is extremely small, leading to the need for extensive structure optimization and parallelization, and for the use of energy storage solutions. However, while the power generated may not be sufficient to power other systems, a practical use-case for triboelectric systems is to act as self-powered sensor systems for detecting motion and touch. Further, because triboelectric systems are based on mechanical touch and friction to create surface charges, these systems are susceptible to mechanical wear, leading to a reduction of the output over a period of time.

**16.4. How does the lithium-ion cell work? What is the main challenge in the development of flexible Li-ion batteries?**

**Ans:** The Li-ion battery operates through the exchange of lithium ions from the anode to the cathode and back through the electrolyte. Both anode and cathode are made using materials that can reversibly incorporate lithium atoms in their lattice structure. The process of incorporation of lithium is called intercalation and the process of removal of lithium is called deintercalation. A typical implementation of Li-ion cell consists of lithium cobalt oxide ( $\text{LiCoO}_2$ ) as the cathode and graphite ( $\text{C}_6$ ) as the anode. During charging, the positive lithium ions from  $\text{LiCoO}_2$  travel through the dielectric, combine with the supplied electrons and intercalate into the graphite electrode as lithium atoms. During discharging, the lithium atoms at the anode dissociate into positive lithium ions and electrons. The electrons are collected by the current collector electrodes, travel across the external circuit, and combine with the positive cobalt ions at the cathode, while the positive lithium ions travel through the electrolyte and intercalate in the cobalt oxide lattice. Electrical work is done by the electrons during this process. The Li-ion batteries provide high energy and power density, low energy leakage, and scalability.

A flexible version of this chemistry is possible if all the components are integrated into a thin-film form on a flexible substrate. Electrolytes are one of the key components of any battery technology. They provide a medium for ion exchange between cathode and anode while discouraging electron exchange. However, they are also the hardest to obtain in a solid-state, thin-film form, marking a key challenge in flexible battery integration. Traditionally, liquid electrolytes are used to provide high ion mobility and good contact with electrode material (wetting). However, the use of liquid electrolytes makes the integration of batteries challenging because of electrolyte encapsulation and leakage issues, particularly upon bending.

**16.5. What is the difference between capacitive energy storage and supercapacitors?**

**Provide the pros/cons for each technology, from a flexible electronics point of view.**

**Ans:** Supercapacitors are capacitive structures that use an electrolyte to create much larger electric fields compared to conventional capacitors. The structure consists of the two electrodes in contact with an electrolyte and uses the buildup of ions in the electrolyte upon application of an external electric potential. The buildup of charge on the metal electrode attracts the ions of opposite polarity from the electrolyte, leading to a buildup of the oppositely charged ions at the metal surface. This double-layer capacitance is used to store energy. The chemistry of the metal electrode and the electrolyte is chosen such that no redox reaction takes place at the metal/electrolyte interface. The buildup of charged ions at the metal electrode surface effectively leads to a very thin (one atomic layer) dielectric between the two charge layers, causing the capacitance of the structure to be extremely high (hence the term “super”capacitor). The high capacitance exhibited by the structure can be used to store much larger amounts of energy compared to regular capacitors. Thus, supercapacitors bridge the gap between MIMcaps and metal-ion batteries, in that they use electrostatic energy storage, but involve ion transporting electrolytes. The key advantage of supercapacitors is that their charge/ discharge rate is much higher than Li-ion batteries. Further, the absence of chemical reactions in their operation leads to much better lifetimes compared to Li-ion batteries. However, a major drawback in the use of supercapacitors for energy storage is their energy density compared to Li-ion batteries. This is mainly because energy is stored only on the surface of the electrode, leaving the bulk volume of the electrode wasted. This is one of the reasons why the creation of thin film-based flexible supercapacitors can be significant. In the electric double-layer supercapacitors, the key factor determining energy storage capacity is the area of the electrodes. Hence, many state-of-the-art implementations of supercapacitors utilize graphene, CNT, and other conductive carbonaceous material electrodes to enhance the electrode surface area

(surface-to-volume ratio). These electrodes can be fabricated in thin-film form using several low-temperature deposition processes on a variety of flexible substrates. However, as in the case of batteries, the key problem for the fabrication of flexible supercapacitors is the integration of an electrolyte.

**17.1. The unstrained resistance of a strain gauge is 10 Ω. If it changes to 10.01 Ω on the application of 20 ppm strain, what is the gauge factor? If all the static resistance values on the Wheatstone bridge are equal to 10 Ω, what is the strain for the voltage output of 5 mV for this strain sensor, if the excitation voltage is 5 V.**

**Ans:**

$$R_o = 10 \, \Omega$$

$$R_1 = 10.01 \, \Omega$$

$$dR = 10.01 - 10 = 0.01 \, \Omega$$

$$\text{Strain} = 20 \, \text{ppm}$$

$$\text{Gauge factor } G = \frac{\frac{dR}{R_o}}{\text{Strain}}$$

$$G = \frac{0.01}{10 * 20}$$

$$G = 5 * 10^{-5}$$

For a Wheatstone bridge,

$$V_{out} = V_{in} * \left[ \frac{R_3}{R_3 + R_g} - \frac{R_2}{R_1 + R_2} \right]$$

$$R_g = 9.96 \, \Omega$$

$$\text{Strain} = \frac{\frac{dR}{R_g}}{G}$$

$$\text{Strain} = \frac{0.04}{10 * 5 * 10^{-5}} = 80$$

**17.2. The temperature coefficient of resistance of platinum is  $0.003927/^{\circ}\text{C}$ . What is the minimum change in temperature that can be detected using a  $100\ \Omega$  sensor of this metal, if the resolution of the resistance measurement is  $0.1\ \Omega$ ?**

**Ans:**

$$R = R_0(1 + \alpha(T - T_0))$$

$$\Delta T = \frac{1}{\alpha} \left( \frac{R}{R_0} - 1 \right)$$

$$\Delta T = \frac{1}{0.003927} \left( \frac{100.1}{100} - 1 \right)$$

$$\Delta T = 0.2546\ ^{\circ}\text{C}$$

**17.3. Describe the structure and working principle of a capacitive pressure sensor. What is the added change in design and advantage of using a touch-mode capacitive pressure sensor?**

**Ans:** Capacitive sensing is widely reported for measuring pressure. In this method, a capacitive structure is fabricated such that one of the metal plates is free to deflect under applied pressure. The deflection in the plate reduces the distance between the two metal plates, causing the capacitance of the structure to increase. The change in capacitance depends on the deflection, which depends on the applied pressure. However, the relationship between the applied pressure and the change in capacitance is not straightforward and depends on the shape of the capacitive structure, the material, and the integration process. For small deflections, the change in capacitance can be approximated as linear. In the case of large pressures, the response is non-linear, but predictable, thus pressure values can be obtained using a device model. For very large pressures, the device architecture is modified so that the deflecting diaphragm is allowed to touch the stationary plate. This can be done without shorting the two electrodes by using a metal/insulator bilayer for fabricating one or both plates. The change in capacitance per unit pressure after the diaphragm has touched is much lower, leading to lower sensitivity, however, the range of measurement increases substantially. This structure is called the “touch mode” capacitive pressure sensor. Capacitive pressure sensors typically feature a movable diaphragm that causes a change in capacitance of the sensor upon application of pressure. In the touch mode sensor, the diaphragm consists of a metal/insulator bilayer and is allowed to touch the substrate to obtain a higher range of sensed pressure.



**17.4. A dielectric elastomer has a breakdown field of 10 MV/m, a dielectric constant of 3, and young's modulus of 10 MPa. We need to create an actuator of area 1 cm<sup>2</sup> that can produce 1 N force using this elastomer. If the thickness of the elastomer is 10 μm, what should be the number of layers in the structure? What is the voltage required for actuation?**

**Ans:** Dielectric constant= 3

Young's modulus= 10 MPa

Breakdown field=10 MV/m

Thickness= 10 μm

Area= 1 cm<sup>2</sup>

Force= 1 N

At maximum actuation, the field in the actuator = 10 MV/m

Thus, Maxwell stress produced  $\sigma = \epsilon E^2 = 2640 \text{ N/m}^2$

For a cross section area of 1 cm<sup>2</sup>, force produced =  $2640 \times 10^{-4} = 0.264 \text{ N}$

Thus, we require four layers of the actuator to create a force of 1 N. The actuation voltage is based on the breakdown voltage. Thus, actuation voltage =  $BD \times t = 100 \text{ V}$ .

**17.5. How can we fabricate a flexible gas sensor? Describe the mechanism of sensing volatile organic compounds using this sensor.**

**Ans:** Gas sensors are typically based on a thin film that changes its characteristics upon exposure to a specific gas. The change in characteristics is then detected using a read-out circuit to determine the concentration of gas in the ambient. For example, tin oxide (SnOx) and zinc oxide (ZnOx) thin films have been used to create sensors for specific volatile organic gases such as methane. These metal oxide thin films adsorb ambient oxygen at the surface which reduces the number of free charge carriers in the material. In the presence of reducing gases, such as methane, the adsorbed oxygen concentration on the surface reduces, increasing the free charge carriers in the thin film, thus increasing the conductivity. The change in resistance of these thin films, thus, provides an indication of the concentration of the reducing gas. Metal oxide nanoparticles are often used to fabricate these thin films to increase the surface-to-volume ratio of the material. In most implementations, the thin films are kept at a specific temperature using microheaters to enhance the adsorption/desorption of gases on the surface and increase sensitivity. These sensors can be fabricated and demonstrated in a flexible form because of the thin-film nature of the sensing material, however, a key constraint in commercial deployment is their encapsulation. Because the sensing thin film needs to be in contact with ambient air, the packaging and encapsulation of gas sensors involves significant integration challenges and requires additional processing to create the window of interaction.

**18.1. Why is it desirable to have stretchable electronic systems? Describe the various ways in which stretchability can be imparted to electronic circuits.**

**Ans:** Manmade intelligent systems are rigid, rectilinear, and fixed-form, while animals and humans have a soft, curvilinear, and free-form exterior. This clear distinction makes the integration of these two systems difficult. This is particularly true for wearable electronic systems (on human or animal skin), or implantable inside a living creature. Wearable systems need to have the stretchability of skin so that they do not impair the free movement of the wearer, and implantable systems may need to grow and change shape as the body of the living being changes with time. These unique requirements create a need for electronics systems that are truly free-form – can be flexed, twisted, stretched, rolled, and so on.

The various ways in which stretchability can be imparted to electronic circuits are stretchability by material and stretchability by design.

**Stretchability by material:** The purpose of designing stretchable electronics, we generally focus on reversible stretchability, thus, we consider the strain at the elastic point, and not the fracture strain of the material. By that standard, most metals that have a reasonably large fracture strain (around 20–40%) will not qualify as stretchable materials because their elastic point is relatively low (2–5%). In general, many polymeric materials like silicones have the capability to undergo large strains, owing to the molecular structure of the material.

**Stretchability by design:** We can impart stretchability in any material system simply by designing it in a particular shape and form. The stress-strain curve of a system depends on both the materials used and the way they are designed. A classic example of this is the simple steel spring. A block of steel of the same dimensions can only stretch reversibly up to 1–2% depending on the type of steel. However, once designed as a spring, the possible reversible

lateral strain can be more than 100%. This transformation is possible because of the unique structure of the spring – a helical spiral around a linear central axis.

**18.2. How does the conductivity of the composite vary with the volume fraction of a conductive filler in a polymer matrix? What is the physical basis for this?**

**Ans:** In polymer composites, the conductivity of the composite varies with the volume fraction of a conductive filler in a polymer matrix such that they retain the stretchability of the polymer matrix while exhibiting the electronic characteristics of the filler material. The most commonly used filler materials are conductive metal nanoparticles, nanotubes, or nanowires which provide conductivity to the polymer matrix, thus creating a stretchable conductor. In some cases, metal ions are implanted in a polymer matrix after it is cured to obtain conductivity in specific parts of the polymer. The presence of conductive particles/nanowires inside the polymer matrix causes conductive paths to be created through the polymer, thus causing the polymer matrix to exhibit metallic conductivity. This is only possible if sufficient conductive filler is added to the polymer matrix such that some conductive paths are created. However, the incorporation of metal fillers changes both the electronic and mechanical properties of the polymer matrix. Thus, although incorporating more fillers may increase the probability of finding conductive paths through the material, the polymer matrix may start to stiffen and lose elasticity.

One of the key mathematical concepts used for determining the variation of conduction in a polymer composite with the addition of filler material is the Percolation Theory. The original theory was designed to discern the probability of forming large, connected clusters inside hypothetical 3D lattices with a given probability of bonding between adjacent sites. The fundamentals of the theory can be applied to determine if at least one conductive path will be obtained from one end of a polymer composite to another, given the random distribution of a specific concentration of the conductive fillers. This is because conduction in polymer composites takes place primarily because of the network created by junctions between adjacent conductive fillers. These junctions can be direct physical contact between adjacent fillers or a

non-contact junction because of the tunnelling of current from one filler to another. Thus, an increase in the volume fraction (volume of fillers compared to the total composite volume) of the conductive fillers should increase the conductivity of the composite. However, this relationship between conductivity and conductive filler volume fraction is not a linear function.

**18.3. Why does a metal spring exhibit reversible stretchability in the linear axis, whereas a metal rod, of the same material, does not?**

**Ans:** A block of steel of the same dimensions can only stretch reversibly up to 1–2% depending on the type of steel. However, once designed as a spring, the possible reversible lateral strain can be in excess of 100%. This transformation is possible because of the unique structure of the spring – a helical spiral around a linear central axis. The radius of the coil and the pitch play a key role in determining the mechanical properties of the spring. We know that when we apply stress to a piece of metal, say a metal wire, the atoms in the metal are displaced causing the overall wire to strain. This strain is typically small for a large applied force (depending on the young’s modulus of the material). Further, in most cases, the strain is not reversible after a certain point. To overcome this problem, we design the spring in such a way that when stress is applied along its axis, it is uniformly distributed along the helical spiral structure. Naturally, this causes the metal to strain. However, because the length of the coil around a certain distance along the linear axis is much larger (because of the circumference of the radial helix), a small strain in the metal along the helical circumference leads to a large apparent strain along the linear axis. This mechanical amplification of strain in the direction of interest is utilized to obtain large reversible strains using materials that have relatively low elastic strains.

**18.4. Give examples of liquid metals. How are they used in stretchable electronics? Why are mercury and francium not used in stretchable electronic applications?**

**Ans:** Metals that have melting points below or near room temperature and are liquid metals are mercury, gallium (29.7°C), francium (27°C), cesium (28.4°C), and rubidium (39.3°C). Mercury has not been used in flexible or stretchable electronic devices because of its toxicity and has a very high surface tension that causes it to form spherical droplets to minimize its surface area. Of these, francium, cesium, and rubidium are not usable for practical consumer electronic devices because francium is radioactive and all three are alkali metals that react explosively with air. Gallium has a melting point of 29.76°C, so is solid at room temperature (25°C) but has very good electrical conductivity. Further, gallium has low toxicity and low reactivity with air, which allows for its use in consumer electronic devices. The melting point of gallium is brought below room temperature by alloying it with other metals such as tin and indium. Two of the most common formulations to this effect are EGaIn (Eutectic gallium indium, 75.5 wt% Ga, 24.5 wt% In, melting point = 15.7°C) and Galinstan (Gallium indium stannum, 68.5 wt% Ga, 21.5 wt% In, 10 wt% Sn, melting point = -19°C). These “liquid metals” have conductivities lower than most conventional metal thin films, however, they are more conductive than polymer composites and are sufficiently conductive for several stretchable electronics applications. Stretchable conductors are generally fabricated by encapsulating these liquid metal droplets inside hollow stretchable elastomer structures.