

Transistor Circuits

Learning Outcomes

This chapter deals with a variety of circuits involving semiconductor devices. These will include bias and stabilisation for transistors, and small-signal a.c. amplifier circuits using both BJTs and FETs. The use of both of these devices as an electronic switch is also considered.

On completion of this chapter you should be able to:

- 1 Understand the need for correct biasing for a transistor, and perform calculations to obtain suitable circuit components to achieve this effect.
- 2 Understand the operation of small-signal amplifiers and carry out calculations to select suitable circuit components, and to predict the amplifier gain figure(s).
- 3 Understand how a transistor may be used as an electronic switch, and carry out simple calculations for this type of circuit.

1 Transistor Bias

In order to use a transistor as an amplifying element it needs to be biased correctly. Although d.c. signals may be amplified, the amplification of a.c. signals is more common. However, the bias is provided by d.c. conditions. Consider a common emitter connected BJT and its input characteristic as illustrated in Fig. 1. The inclusion of resistor R_C is not required at this stage, but would be present in any practical amplifier circuit, so is shown merely for completeness. This resistor is called the collector load resistor.

With the switch in position '1' the value of forward bias V_{BEQ} has been chosen such that it coincides with the centre of the linear portion of the input characteristic. This point on the characteristic is identified by the letter Q, because, without any a.c. input signal connected, the transistor is said to be in its quiescent state. Under this condition the base current will be I_{BQ} with the corresponding values of collector and emitter currents being I_{CQ} and I_{EQ} respectively. The use of capital letters in the subscripts indicates d.c. quantities, and the letter Q that they are quiescent values.

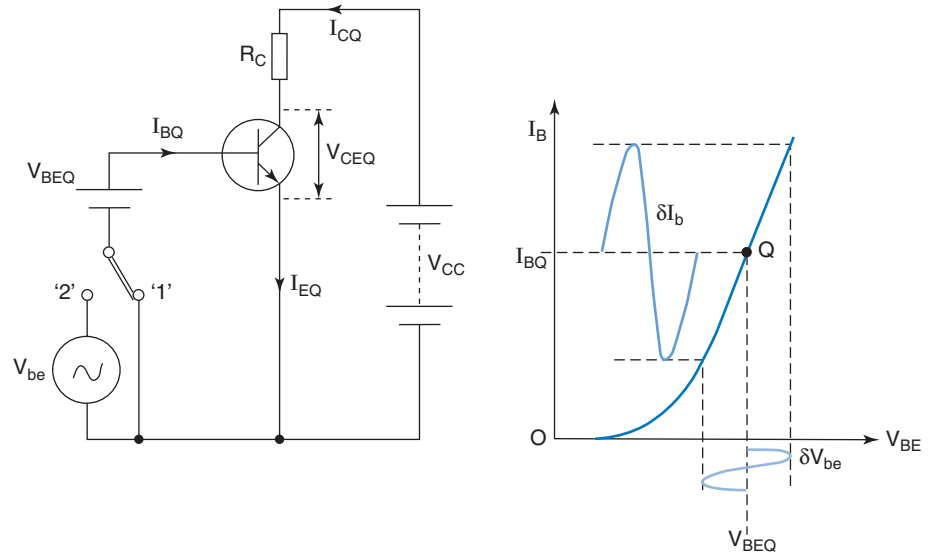


Fig. 1

Consider now what happens when the switch is moved to position '2', thus connecting the a.c. signal generator between base and emitter. The a.c. signal V_{be} (note the use of lower case letters to indicate an a.c. quantity) from the generator would normally vary about 0V, but it will now be superimposed on the quiescent d.c. bias level V_{BEQ} . Thus the effective bias voltage will vary in sympathy with the input signal, causing a corresponding variation of the base current about its quiescent d.c. level as shown. Due to transistor action there will be corresponding variations of both collector and emitter currents about their quiescent values.

Figure 2 shows the effect when a different d.c. bias voltage, and hence different Q point, is selected.

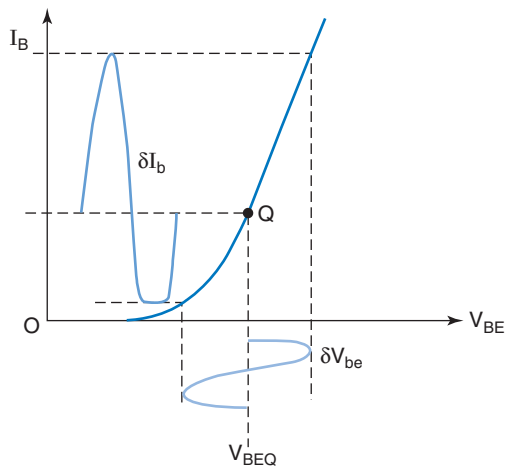


Fig. 2

The sinusoidal variation of V_{be} will again cause variation of I_b , but due to the curvature at the bottom of the characteristic the resulting base current will be distorted as shown. This same distortion will be reflected in the collector and emitter currents also. This distortion needs to be avoided, so the bias voltage and hence Q point must be carefully chosen.

The provision of V_{CC} by means of a battery or other d.c. source will always be required, but the provision of the forward bias voltage V_{BEQ} by a second battery or other d.c. source is inconvenient. There are a number of ways of providing the required bias conditions without the need for a second source of emf.

2 A Simple Bias Circuit

In the circuit of Fig. 3 the required quiescent base current I_{BQ} is provided from V_{CC} via resistor R_B .

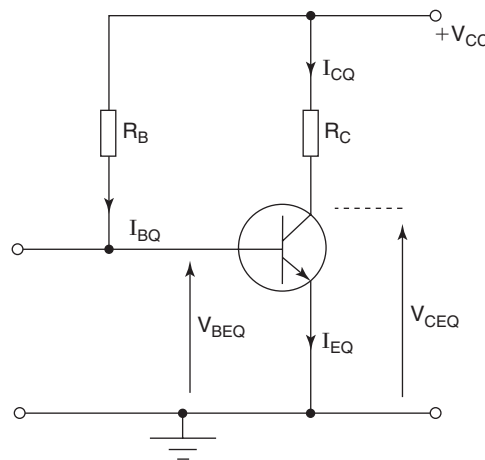


Fig. 3

The current flowing through R_B depends upon the p.d. across it, which will be $(V_{CC} - V_{BEQ})$ volt. Thus if we know the required values for I_{BQ} and V_{BEQ} by studying the input characteristic, the value for R_B may be calculated as follows.

$$R_B = \frac{(V_{CC} - V_{BEQ})}{I_{BQ}} \text{ ohm} \quad (1)$$

In practice, $V_{CC} \gg V_{BEQ}$, so the above equation is often simplified to

$$R_B = \frac{V_{CC}}{I_{BQ}} \text{ ohm} \quad (2)$$

This approximation is valid since when selecting a value for R_B the nearest preferred value would have to be used. This is demonstrated in the following example.

Worked Example 1

Q A simply biased transistor circuit is shown in Fig. 4. The required quiescent values for base current and base-emitter voltage are $60\ \mu\text{A}$ and 0.8V respectively. Determine a suitable value for resistor R_B .

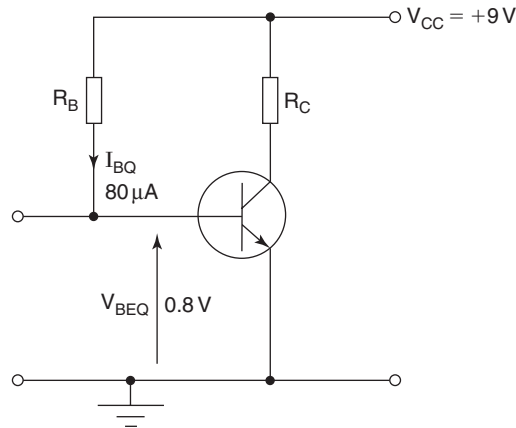


Fig. 4

A

$$V_{CC} = 9\text{ V}; I_{BQ} = 60 \times 10^{-6}\text{ A}; V_{BEQ} = 0.8\text{ V}$$

Using equation (2) we have

$$R_B = \frac{(V_{CC} - V_{BEQ})}{I_{BQ}} \text{ ohm} = \frac{(9 - 0.8)}{60 \times 10^{-6}}$$

$$R_B = 137\text{ k}\Omega \text{ Ans}$$

Using the approximation of equation (2) gives

$$R_B = \frac{V_{CC}}{I_{BQ}} \text{ ohm} = \frac{9}{0.8}$$

$$R_B = 150\text{ k}\Omega \text{ Ans}$$

Now, the nearest preferred value would be $150\text{ k}\Omega$, so the use of equation (2) is justified.

Although this bias circuit has the advantage of simplicity, it cannot overcome the problem of the bias and hence Q point varying with temperature change, and the even more serious problem of thermal runaway.

3 Thermal Runaway

When the transistor is operating in a circuit, the collector current will tend to cause a temperature increase, with a consequent increase of

transistor current gain h_{FB} . For example, assume that h_{FB} increases from 0.98 to 0.99 under this condition. This is an increase of only about 1%, and so will result in only a very small increase of collector current. For this reason, if the transistor is connected in the common base configuration it will be relatively stable, and the simple bias circuit described will usually be acceptable.

Consider now the effect of the same increase of temperature when this same transistor is connected in the common emitter configuration. h_{FB} will increase from 0.98 to 0.99 as before, but the effect on h_{FE} is more dramatic as shown below.

$$\text{When } h_{FB} = 0.98; \quad h_{FE} = \frac{h_{FB}}{1 - h_{FB}} = \frac{0.98}{0.02} = 49$$

$$\text{When } h_{FB} = 0.99; \quad h_{FE} = \frac{0.99}{0.01} = 99$$

Thus for the same temperature rise the transistor current gain has more than doubled, with a corresponding increase in collector current. This will result in a further increase in temperature, a further small increase in h_{FB} , and a further massive increase in h_{FE} , etc.

The process is a cumulative one known as thermal runaway which will result in the rapid destruction of the transistor. Since the runaway condition is the result of a rapid increase of collector current, then some means of preventing this needs to be employed.

4 Bias with Thermal Stabilisation

One simple method of providing a degree of thermal stability is to connect the bias resistor directly to the collector, as shown in Fig. 5.

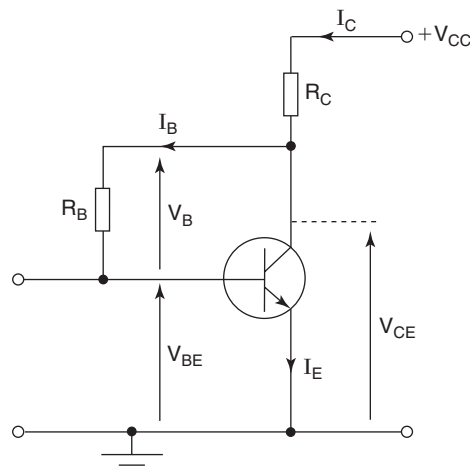


Fig. 5

In this circuit the p.d. across R_B is dependent upon the potential at the collector. With a temperature rise the collector current will tend to rise. This increase will cause increased voltage drop across resistor R_C , resulting in a lower potential at the collector, which in turn will tend to reduce base current I_B . Any tendency for base current to fall will be reflected by the same tendency in collector current. Thus we have gone full circle, whereby the original tendency for I_C to increase has been counteracted.

Although this circuit will give good stability for a transistor connected in common base, it may not be entirely satisfactory for the common emitter mode, particularly when the operating conditions elevate the temperature still further. For this reason a more effective method is more often employed, as described in the next section.

5 Three-resistor Bias and Stabilisation

A circuit showing this method of biasing is shown in Fig. 6 and this is by far the most common biasing technique employed in practice.

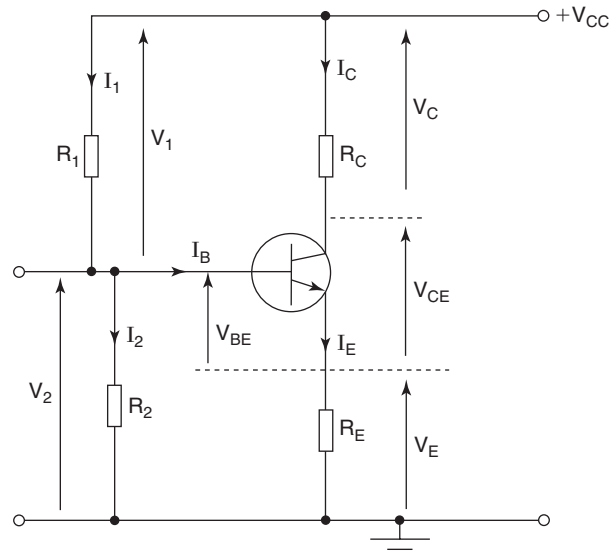


Fig. 6

The potential divider chain formed by R_1 and R_2 provides a fixed potential V_2 to the base of the transistor. Resistor R_E is involved in both providing the bias and the thermal stability. The potential at the emitter is V_E , where $V_E = I_E R_E$ volt.

The emitter-base bias voltage will be the difference between the potentials at these two electrodes, so $V_{BE} = (V_2 - V_E)$ volt. Thermal stability is achieved as follows.

As a result of temperature rise, I_C will tend to rise. This will be mirrored by a corresponding increase in emitter current I_E . However, the base potential V_2 is fixed, so the overall bias V_{BE} will tend to decrease, which in turn will tend to reduce I_C . Once more the system has gone full circle such that the original tendency for collector current to increase has been counteracted. This effect is illustrated below, where the arrows show the tendencies for the various quantities to increase or decrease.

$$\begin{array}{ccccccc} \uparrow & \uparrow & \uparrow & \text{(bias)} & & & \\ I_C, & I_E, & V_E, & (V_2 - V_E), & I_B, & I_C & \\ & & & \downarrow & \downarrow & \downarrow & \end{array}$$

When calculating suitable values for the bias components the following points should be borne in mind.

- (a) For good thermal stability the p.d. across R_E should be about $V_{CC}/10$ volt.
- (b) The value of R_2 should be at least $10 \times R_E$ ohm.
- (c) The current I_1 through R_1 should be approximately 10 to $20 \times I_{BQ}$.
- (d) The collector-emitter voltage V_{CE} should be approximately $V_{CC}/2$ volt.

These points are best illustrated by means of the following example.

Worked Example 2

- Q** For the circuit of Fig. 6 the transistor has a current gain, $h_{FE} = 80$ and the collector supply voltage, $V_{CC} = +10\text{V}$. The required bias conditions are $V_{BE} = 0.7\text{V}$, and $I_C = 1\text{mA}$. Determine suitable values for resistors R_1 , R_2 , R_E and R_C .

A

$$V_{CC} = 10\text{V}; I_C = 10^{-3}\text{A}; V_{BE} = 0.7\text{V}; h_{FE} = 80$$

$$\text{Since } I_E \approx I_C, \text{ then } I_E = 1\text{mA}$$

$$\text{and if } V_E = V_{CC}/10, \text{ then } V_E = 1\text{V}$$

$$\text{hence, } R_E = \frac{V_E}{I_E} \text{ ohm} = \frac{1}{10^{-3}}$$

$$R_E = 1\text{ k}\Omega \text{ Ans}$$

$$\text{if } R_2 = 10 R_E, \text{ then}$$

$$R_2 = 10\text{ k}\Omega \text{ Ans}$$

$$V_{BE} = (V_2 - V_E) \text{ volt}$$

$$\text{so, } V_2 = V_{BE} + V_E = 0.7 + 1 = 1.7\text{V}$$

$$I_2 = \frac{V_2}{R_2} \text{ amp} = \frac{1.7}{10^4}$$

$$\text{and, } I_2 = 0.17\text{ mA}$$

$$I_B = \frac{I_C}{h_{FE}} = \frac{10^{-3}}{80}$$

$$I_B = 12.5\ \mu\text{A} \text{ or } 0.0125\text{ mA}$$

$$I_1 = I_2 + I_B = 0.17 + 0.0125 = 0.1825\text{ mA}$$

$$V_1 = V_{CC} - V_2 \text{ volt} = 10 - 1.7 = 8.3 \text{ V}$$

$$R_1 = \frac{V_1}{I_1} \text{ ohm} = \frac{8.3}{0.1825 \times 10^{-3}}$$

$$R_1 = 46 \text{ k}\Omega, \text{ and the nearest preferred value is } 47 \text{ k}\Omega \text{ Ans}$$

$$V_C = V_{CC} - (V_E + V_{CE}) \text{ volt} = 10 - (1 + 5) \text{ assuming that } V_{CE} = V_{CC}/2$$

$$V_C = 4 \text{ V}$$

$$R_C = \frac{V_C}{I_C} \text{ ohm} = \frac{4}{10^{-3}}$$

$$R_C = 4 \text{ k}\Omega, \text{ and the nearest preferred value is } 3.9 \text{ k}\Omega \text{ Ans}$$

6 Biasing Circuits for FETs

In general, FETs are much simpler devices than BJTs, and since the gate draws negligible current the bias arrangements can also be simpler. FETs also have the advantage that they tend not to suffer thermal runaway, though change in temperature can cause drift of the Q point.

The simplest arrangement for a common source circuit is shown in Fig. 7. The resistor R_D is equivalent to the collector resistor R_C in the BJT circuit.

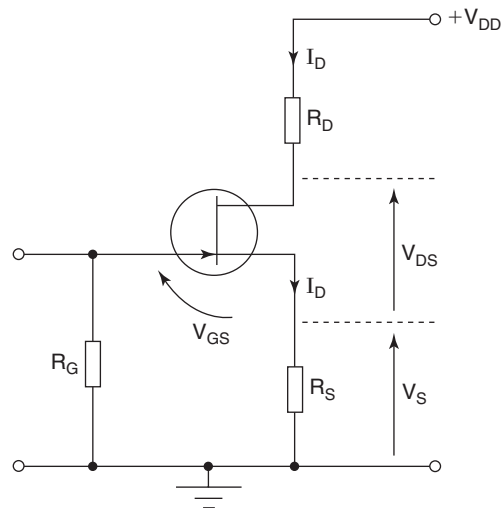


Fig. 7

Essentially, the gate-source bias voltage is provided by R_S . Resistor R_G will be a high value resistor, typically in megohms, which is used to connect the 0V rail to the gate. Now, you may well ask the question, how can a large value resistor act as a direct connection between the 0V rail and the gate? The answer is very simple. Since the gate draws negligible current there will be negligible current through R_G , hence negligible voltage drop across it, so both ends of the resistor must be at the same potential, i.e. 0V. The FET itself has a very high input impedance, and therefore will have almost no loading effect on a signal

source connected between gate and source. In order not to compromise this effect, resistor R_G is chosen to have a high value.

Drain current I_D flowing through R_S results in voltage V_S being developed across it. Thus the potential at the source will be positive with respect to the gate, which is the required bias condition.

If full bias stabilisation is required, then a three-resistor method similar to that used for the BJT may be employed, and such a circuit is shown in Fig. 8.

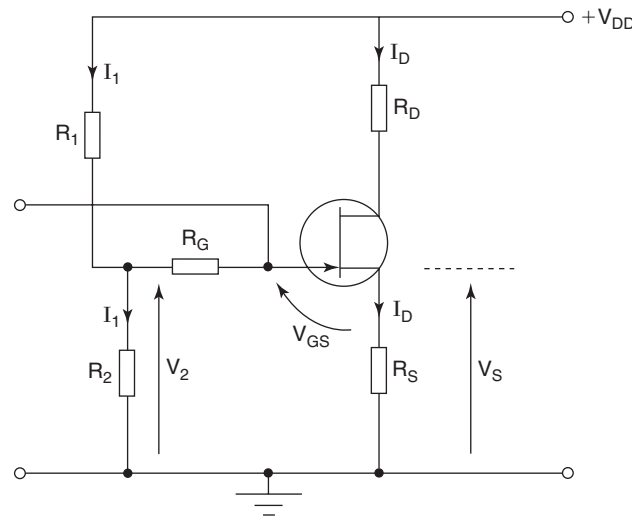


Fig. 8

In this circuit, the bias voltage is provided by R_2 and R_S , since $V_{GS} = (V_2 - V_S)$ volt. Resistor R_G performs a similar function to that in the previous circuit, i.e. to connect potential V_2 to the gate. The stabilising action will be very similar to that for the BJT circuit, in that increase of I_D due to temperature will increase V_S . This has the effect of making the gate more negative with respect to the source, i.e. the forward bias is reduced and I_D is reduced.

7 Small Signal A.C. Amplifiers

A simply biased common emitter amplifier circuit is shown in Fig. 9. On this diagram both d.c. (biasing conditions) and a.c. (signal conditions) quantities have been identified. The use of upper case letters, such as V_{CE} , identify the d.c. quantities, and the lower case letters, such as i_b , identify the a.c. quantities.

The purpose of the collector load resistor R_C is to develop an a.c. output voltage when the a.c. component of collector current, i_c , flows through it. Capacitors C_1 and C_2 are known as coupling capacitors. C_1 allows the a.c. input signal to be connected to the base, but will

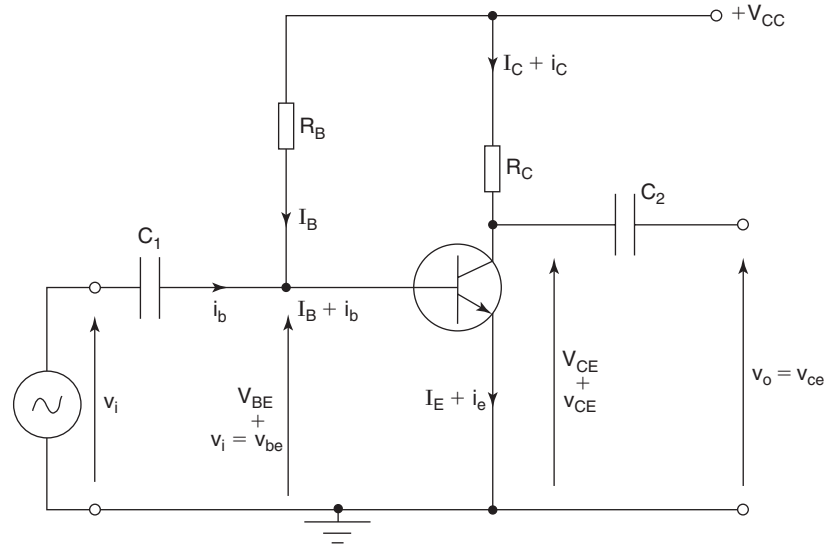


Fig. 9

block any d.c. level (normally 0V) from the signal generator affecting the d.c. bias conditions of the transistor. Similarly, C_2 couples the a.c. signal developed across R_C to the output terminals, but prevents the quiescent collector voltage from affecting the output waveform. The values of these capacitors are chosen so that they will have very low reactance at the signal frequency, and therefore are virtually ‘transparent’ to the a.c. signal, i.e. they will have imposed negligible voltage drop. The effect of the capacitors on the various currents and voltages is illustrated in Fig. 10.

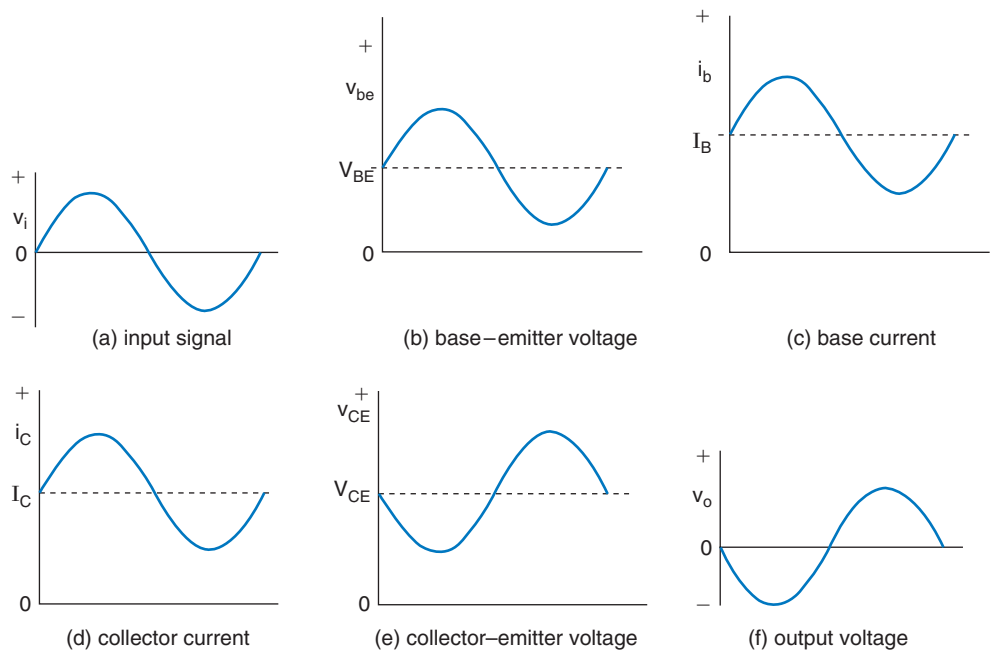


Fig. 10

Notes:

- 1 The amplitude of $V_{be} = V_i$, but capacitor C_1 has prevented the 0V level of the signal generator from altering the transistor bias V_{BE} .
- 2 Observe that v_{ce} and hence output voltage v_o is phase-inverted (is antiphase to) the input signal v_i .
- 3 The amplitude of the output $v_o = v_{ce}$, and capacitor C_2 has prevented the quiescent d.c. level V_{CE} from being connected to the output terminals.

With reference to Note 2 above, the reason for the phase inversion is explained as follows. The potential at the collector depends upon the value of current flowing through R_C . From Fig. 10(d) it can be seen that I_C goes more positive in the first half cycle, in response to the input signal. This will result in a larger p.d. across R_C , but since the upper end of this resistor is tied to $+V_{CC}$, then the potential at the collector end must fall. Thus during this half cycle v_{ce} will decrease from its quiescent value. In the next half cycle i_c decreases, so the potential at the collector rises and we have phase inversion.

With R_C in the amplifier circuit an output voltage has been developed. Consider now how we can utilise this so as to analyse the performance of the amplifier. Firstly let us apply Kirchhoff's voltage law between the power supply rails (V_{CC} and 0V), taking the route through R_C and the transistor, for the circuit of Fig. 9.

$$V_{CC} = I_C R_C + V_{CE} \text{ volt}$$

$$\text{when } I_C = 0; \quad \text{then } V_{CE} = V_{CC} \text{ volt} \dots\dots\dots[1]$$

$$\text{when } V_{CC} = 0; \quad \text{then } I_C = \frac{V_{CC}}{R_C} \text{ amp} \dots\dots\dots[2]$$

The conditions where $I_C = 0$ and $V_{CC} = 0$ are two points on the axes of the transistor's output characteristics, and the straight line joining these two points is known as the d.c. or static load line for resistor R_C . A typical set of characteristics with the d.c. load line drawn on it is shown in Fig. 11. The slope of the load line is $-1/R_C$ mA/V. The minus sign is due to the negative slope.

Where the load line intersects the characteristic for I_{BQ} gives the Q point for the transistor. Indeed this gives an alternative method for determining a suitable Q point without having to refer to the input characteristic. Bearing in mind that V_{CEQ} needs to be $\approx V_{CC}/2$ volt, then the nearest intersection that corresponds to this requirement will be a suitable choice.

The intersections of the load line with the characteristics shows the limitations imposed on the excursions of collector current (δI_c) and voltage (δV_{ce}) for a given excursion of base current (δI_b). From this we can determine the *amplifier* current and voltage gains, which are defined as follows.

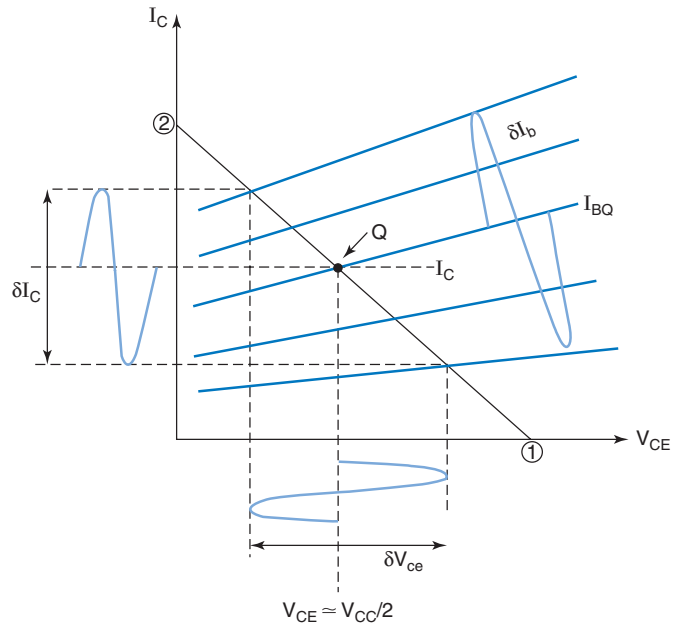


Fig. 11

$$\text{Amplifier current gain, } A_i = \frac{\delta I_c}{\delta I_b} \quad (3)$$

$$\text{Amplifier voltage gain, } A_v = \frac{\delta V_{ce}}{\delta V_{be}} \quad (4)$$

$$\text{and amplifier power gain, } A_p = A_i \times A_v \quad (5)$$

The variation δV_{be} corresponds to the a.c. input signal excursion δV_i . Note that the *amplifier* current gain will *always* be less than the transistor current gain h_{FE} , because the latter is defined with V_{CE} constant. Also note that the amplifier power gain refers to the ratio of the *signal* output power to the *signal* input power. When the comparatively large power input from the V_{CC} power supply is taken into account, the overall efficiency of such an amplifier circuit in terms of power output to the total power input will be found to be less than 25%.

The a.c. Equivalent Circuit The circuit of Fig. 9 may be redrawn in terms of what the a.c. signals will 'see'. In this case the coupling capacitors C_1 and C_2 are transparent to a.c. and therefore act as short circuits to a.c. signals. The battery supplying V_{CC} will also behave as if it were a large value capacitor, and therefore act as a short-circuit to a.c. signals. Considering a battery in this way is quite valid when you consider what it is comprised of—a set of large oppositely charged plates separated by an electrolyte (insulator), i.e. the same construction as a capacitor! Any other form of d.c. supply used to provide V_{CC} will have the same effect. The result as far as a.c. signals are concerned is that

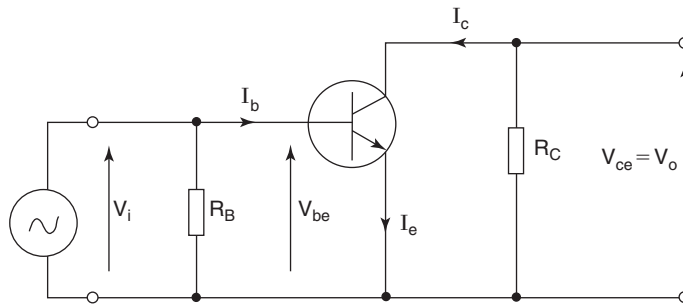


Fig. 12

the $+V_{CC}$ rail is directly connected to the 0V rail. Thus the upper ends of both R_B and R_C are effectively connected to the common 0V rail. The a.c. equivalent circuit will therefore be as shown in Fig. 12.

Worked Example 3

Q For the amplifier circuit of Fig. 13 an input signal of 300 mV pk-pk causes the base current to vary by $80 \mu\text{A}$ pk-pk about its quiescent value of $60 \mu\text{A}$. The output characteristics for the transistor are given in Fig. 14.

Draw the load line on these characteristics and hence determine

- the transistor current gain, h_{FE} ,
- the amplifier current gain, A_I ,
- the amplifier voltage and power gains, A_V and A_{p_r} , and
- sketch the a.c. equivalent circuit.

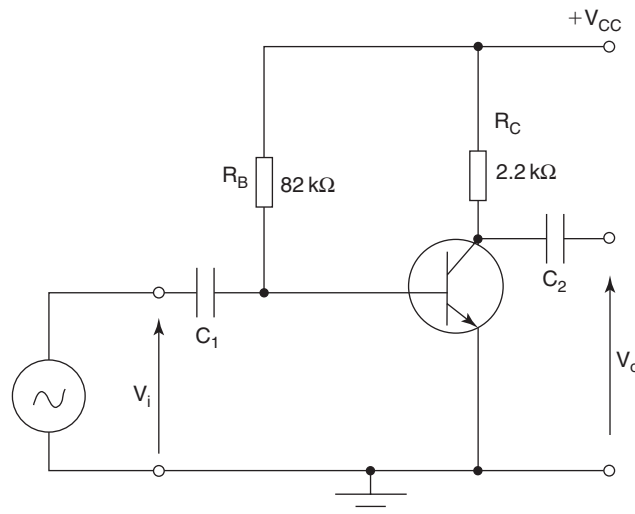


Fig. 13

A

$$\delta V_i = 0.3 \text{ V pk-pk}; \delta I_b = 80 \times 10^{-6} \text{ A pk-pk}; I_{BQ} = 60 \times 10^{-6} \text{ A}; V_{CC} = 9 \text{ V};$$

$$R_C = 2.2 \times 10^3 \Omega; R_B = 82 \times 10^3 \Omega$$

$$\text{For the load line: } V_{CC} = I_C R_C + V_{CE} \text{ volt}$$

when $I_C = 0$; $V_{CE} = V_{CC} = 9 \text{ V}$ [1]

when $V_{CE} = 0$; $I_C = \frac{V_{CC}}{R_C} \text{ amp} = \frac{9}{2.2} = 4.1 \text{ mA}$ [2]

Joining these two points by a straight line gives the load line as shown in Fig. 14 and its intersection with $I_B = 60 \mu\text{A}$ gives the Q point, with $V_{CEQ} = 4.6 \text{ V}$.

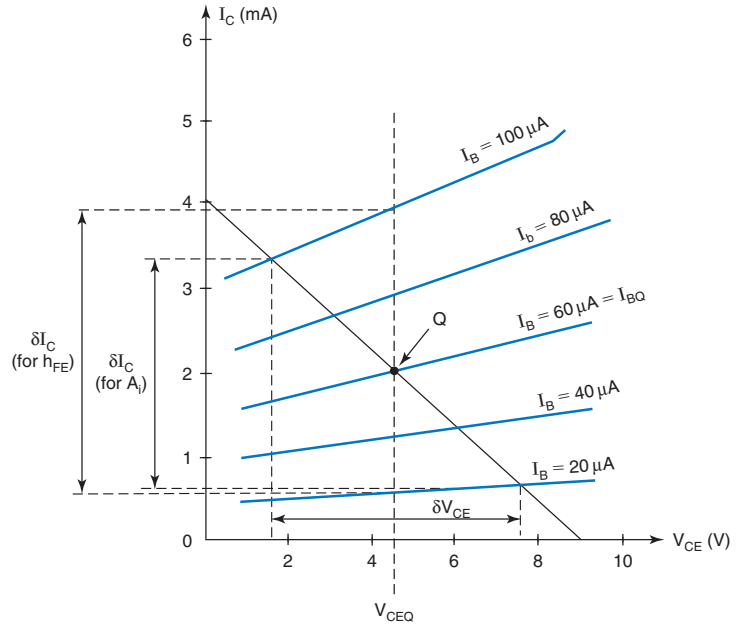


Fig. 14

(a) $h_{FE} = \frac{\delta I_C}{\delta I_B} \text{ (with } V_{CE} = 4.6 \text{ V)} = \frac{(3.95 - 0.55) \times 10^{-3}}{(100 - 20) \times 10^{-6}}$
 $h_{FE} = 42.5 \text{ Ans}$

(b) For amplifier gains, the excursions of I_C and V_{ce} are determined by the intercepts with the load line.

$\delta I_C = (3.35 - 0.62) \text{ mA} = 2.73 \text{ mA pk-pk}$

$\delta I_b = 80 \mu\text{A pk-pk}$

$A_i = \frac{\delta I_C}{\delta I_b} = \frac{2.73 \times 10^{-3}}{80 \times 10^{-6}}$

$A_i = 34.1 \text{ Ans}$ Note that this figure is $< h_{FE}$.

(c) $\delta V_{ce} = (7.6 - 1.6) \text{ V} = 7 \text{ V pk-pk}$

$\delta V_{be} = 0.3 \text{ V pk-pk}$

$A_V = \frac{\delta V_{ce}}{\delta V_{be}} = \frac{7}{0.3}$

$A_V = 23.3 \text{ Ans}$

$A_p = A_i \times A_V = 34.1 \times 23.3$

$A_p = 796 \text{ Ans}$

(d) The a.c. equivalent circuit will be as shown in Fig. 15.

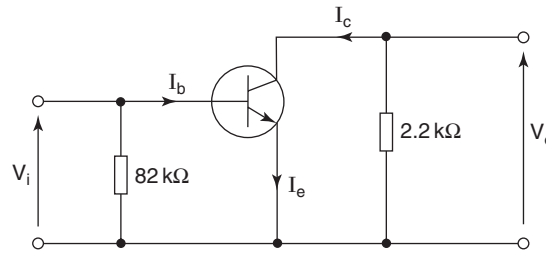


Fig. 15

Affect of External load In the previous example it has been assumed that no current was drawn from the circuit at the output terminals, i.e. any external load connected there has an infinite input impedance. The result was that both the d.c. quiescent collector current and the a.c. component of this current both flowed through R_C only, and the d.c. load line limited the excursions of the a.c. components of current and voltage. In practice, any load connected to the output terminals will have a finite impedance, and will therefore offer another path for the a.c. signal via C_2 . Due to the d.c. blocking action of this capacitor, the d.c. conditions will not be affected.

Considering the circuit for the previous example, where a $10\text{ k}\Omega$ external load, R_L , is now connected between the output terminals. The a.c. equivalent will now be as shown in Fig. 16.

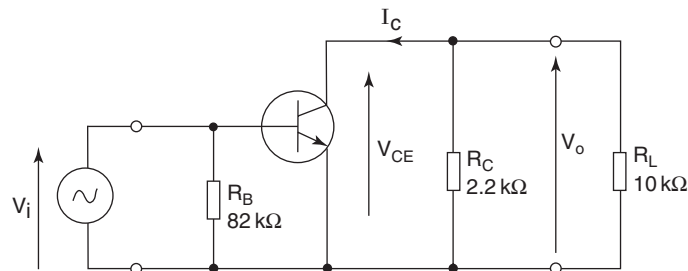


Fig. 16

The effective a.c. load, R_e , will be the parallel combination of R_C and R_L .

$R_e = \frac{R_C R_L}{R_C + R_L}$ ohm and the a.c. load line will have a slope of $-1/R_e$ amp/volt passing through the Q point already established by the d.c. load line. The following example shows how this will affect the analysis of the amplifier circuit.

Worked Example 4

Q Using the same set of output characteristics as for Example 4, and adding a $10\text{ k}\Omega$ external load to the circuit of Fig. 13, calculate the amplifier current, voltage and power gains.

A

The d.c. load line would be determined and plotted in exactly the same way as before, and this is shown in Fig. 17.

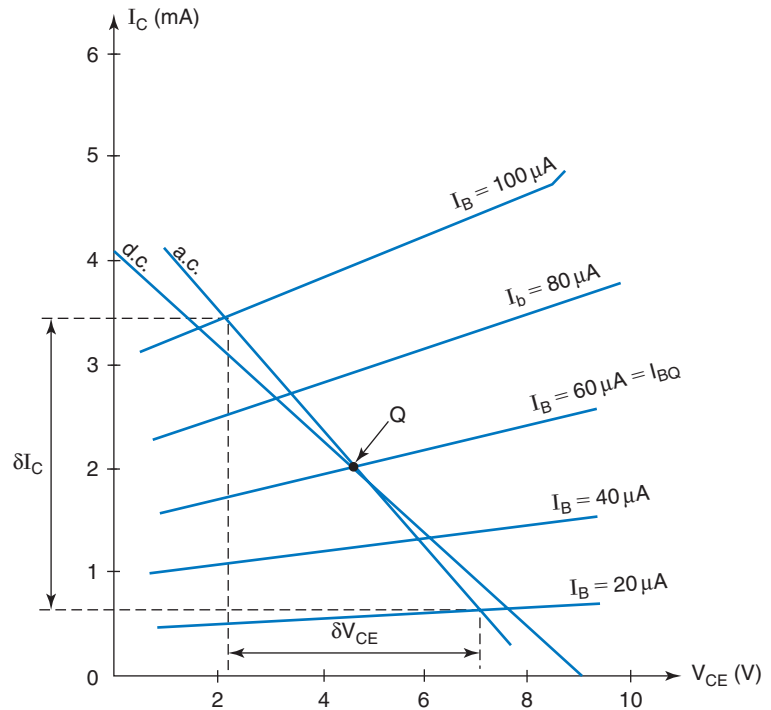


Fig. 17

$$\text{a.c. load line: } R_e = \frac{R_C R_L}{R_C + R_L} \text{ ohm} = \frac{10 \times 2.2}{10 + 2.2} \text{ k}\Omega$$

$$R_e = 1.8 \text{ k}\Omega \text{ and the slope} = \frac{-1}{1.8} \text{ mA/V} = -0.56 \text{ mA/V}$$

Now we know that the a.c. load line will pass through the Q point; so starting at this point, if we drop vertically by 0.56 mA and then move to the right by 1 V, we will have a second point through which the a.c. load line passes. However, this second point is very close to the Q point, so to improve the accuracy, double up the above figures, i.e. starting at the Q point drop down 1.12 mA and move right 2 V. The resulting a.c. load line will then be plotted as in Fig. 17, and the excursions of I_c and V_{ce} determined from the intersections with it, as follows.

$$\delta I_c = (3.45 - 0.6) \text{ mA} = 2.85 \text{ mA pk-pk}$$

$$A_i = \frac{\delta I_c}{\delta I_b} = \frac{2.85 \times 10^{-3}}{80 \times 10^{-6}}$$

$$A_i = 35.6 \text{ Ans}$$

$$\delta V_{ce} = (7.1 - 2.2) \text{ V} = 4.9 \text{ V pk-pk}$$

$$A_v = \frac{\delta V_{ce}}{\delta V_{be}} = \frac{4.9}{0.3}$$

$$A_v = 16.3 \text{ Ans}$$

$$A_p = A_i \times A_v = 35.6 \times 16.3$$

$$A_p = 580 \text{ Ans}$$

8 Three-resistor-biased Amplifier Circuit

When this circuit is employed there will be implications for both the d.c. and the a.c. load lines. A typical circuit is shown in Fig. 18, where an external load resistor is also included.

d.c. load line: applying Kirchhoff's voltage law as before:

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \text{ volt}$$

but $I_C \approx I_E$, so

$$V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

and, $V_{CC} = I_C (R_C + R_E) + V_{CE}$

when $I_C = 0$; $V_{CE} = V_{CC}$ (as before) [1]

when $V_{CE} = 0$; $I_C = \frac{V_{CC}}{(R_C + R_E)}$ amp [2]

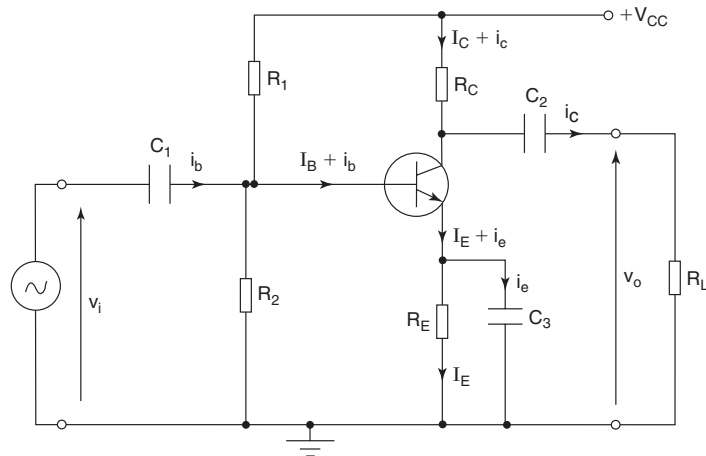


Fig. 18

The d.c. load line will now have a slope of $-1/(R_C + R_E)$ volt/amp, and when plotted on the output characteristics will establish the Q point.

a.c. load line: the effective a.c. load, $R_e = \frac{R_C R_L}{R_C + R_L}$ ohm

and the a.c. load line will have a slope = $-1/R_e$ amp/volt, passing through the Q point, as in the previous example.

The a.c. equivalent circuit is shown in Fig. 19.

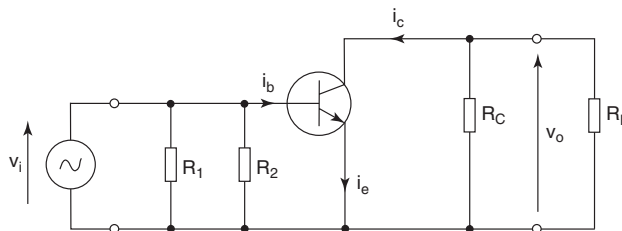


Fig. 19

Worked Example 5

Q For the circuit of Fig. 18 let the component values be $R_C = 3.3\text{ k}\Omega$; $R_E = 560\ \Omega$; $R_L = 10\text{ k}\Omega$ and $V_{CC} = +10\text{ V}$. You may assume that the capacitors have negligible reactance at the signal frequency. The transistor output characteristics are as in Fig. 20, and the input signal generator causes the base current to vary by $80\ \mu\text{A}$ pk-pk about its quiescent value.

- (a) Plot the d.c. load line and hence determine a suitable Q point.
- (b) Plot the a.c. load line and hence determine the amplifier current gain.

A

$$R_C = 3.3 \times 10^3\ \Omega; R_E = 560\ \Omega; R_L = 10^4\ \Omega; V_{CC} = 10\text{ V}; \delta I_b = 80 \times 10^{-6}\ \text{A}$$

(a) $V_{CC} = I_C(R_C + R_E) + V_{CE}$ volt

when $I_C = 0$; $V_{CE} = V_{CC} = 10\ \text{V}$ [1]

when $V_{CE} = 0$; $I_C = \frac{V_{CC}}{R_C + R_E}$ amp = $\frac{10}{3.86}$ mA [2]

$$I_C = 2.6\ \text{mA}$$

This load line is then plotted as shown in Fig. 20, and since, for practical purposes, V_{CEQ} should be about $V_{CC}/2$ volt, the Q point is chosen where the d.c. load line intersects with the $I_B = 60\ \mu\text{A}$ graph. This gives $V_{CEQ} = 4.7\text{ V}$.

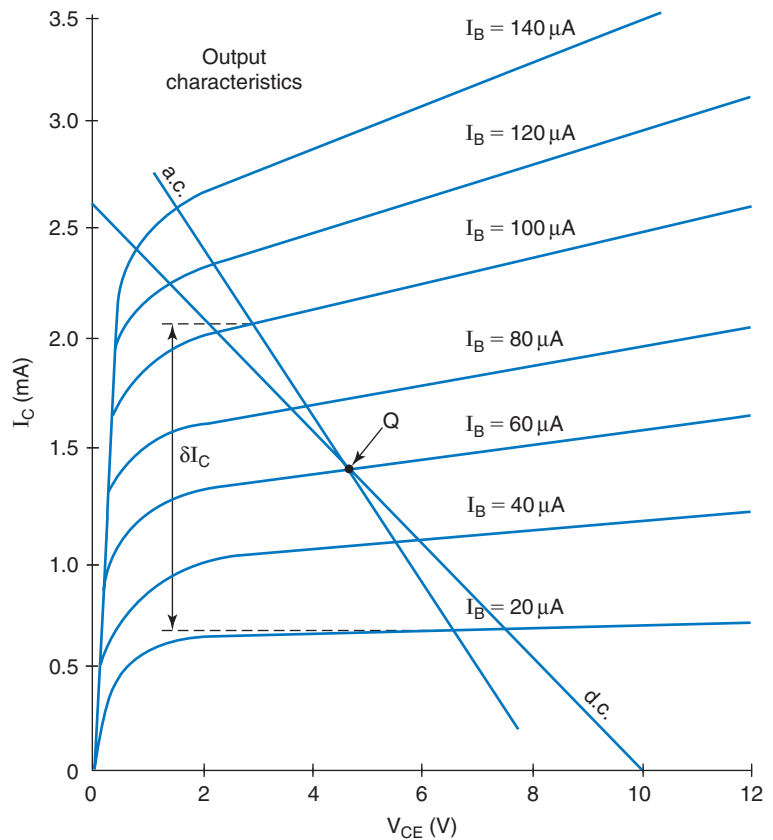


Fig. 20

(b) **a.c. loadline:** $R_e = \frac{R_C R_L}{R_C + R_L} \text{ ohm} = \frac{33}{13.6} \text{ k}\Omega$
 $R_e = 2.48 \text{ k}\Omega$

slope = $\frac{-1}{2.48} \text{ mA/V} = -0.4 \text{ mA/V}$ (use -1.2 mA/3V)

and the load line is plotted with this slope passing through the Q point as shown.

$\delta I_b = 80 \mu\text{A}$ pk-pk about $I_B = 60 \mu\text{A}$

so, $\delta I_c = (2.05 - 0.65) \text{ mA} = 1.4 \text{ mA}$ pk-pk

$A_i = \frac{\delta I_c}{\delta I_b} = \frac{1.4 \times 10^{-3}}{80 \times 10^{-6}}$

$A_i = 17.5$ **Ans**

9 FET Small-signal Amplifier

A typical FET signal amplifier circuit is shown in Fig. 21.

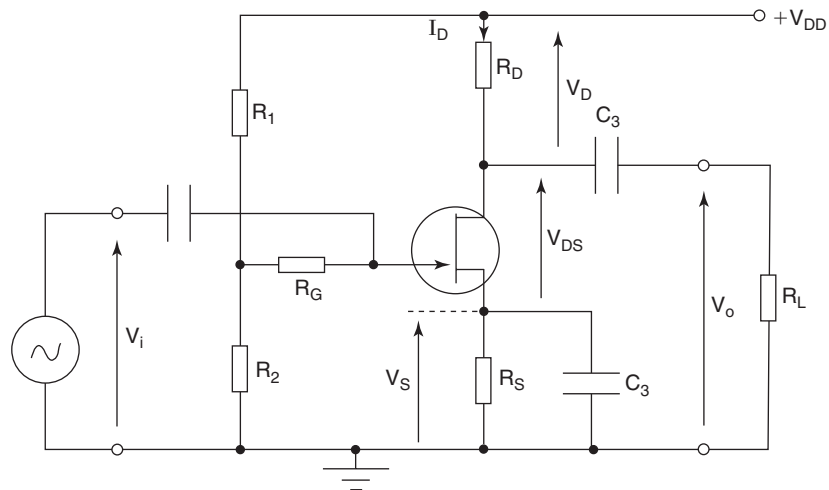


Fig. 21

The amplifier voltage gain, A_v , may be determined from load lines plotted on the output characteristics in a similar manner to that for the BJT amplifier.

d.c. load line: $V_{DD} = V_D + V_{DS} + V_S$ volt

where $V_D = I_D R_D$ and $V_S = I_D R_S$ volt

$V_{DD} = I_D (R_D + R_S) + V_{DS}$ volt

when $I_D = 0$; $V_{DS} = V_{DD}$ [1]

when $V_{DS} = 0$; $I_{DS} = \frac{V_{DD}}{R_D + R_S}$ amp [2]

Thus the d.c. load line may be plotted and a suitable Q point selected.

a.c. load line: the effective a.c. load, $R_e = \frac{R_D R_L}{R_D + R_L}$ ohm

and this load line will have a slope of $-1/R_e$ amp/volt.

Both load lines are shown plotted on Fig. 22.

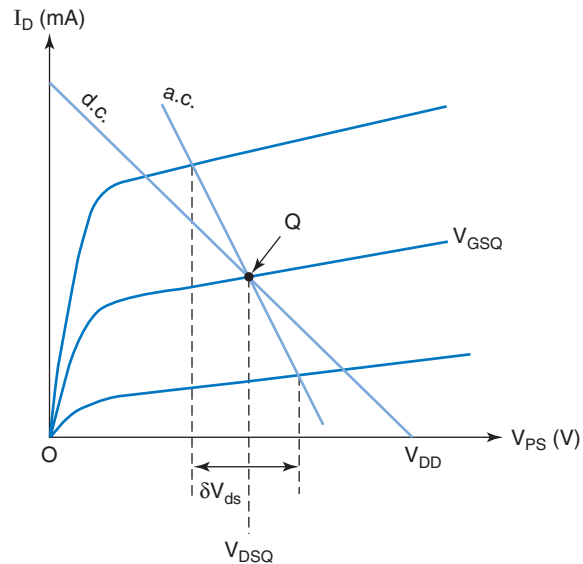


Fig. 22

Worked Example 6

Q The FET used in the circuit of Fig. 23 has characteristics as shown in Fig. 24.

- (a) From the characteristics, determine:
- (i) the mutual conductance, g_m , when $V_{DS} = 12\text{V}$, and
 - (ii) the drain-source resistance, r_{DS} for $V_{GS} = -3.5\text{V}$.

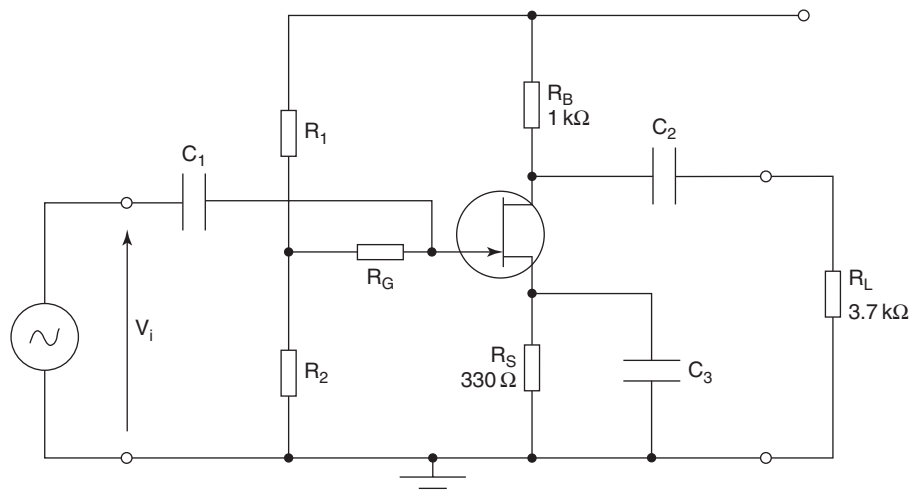


Fig. 23

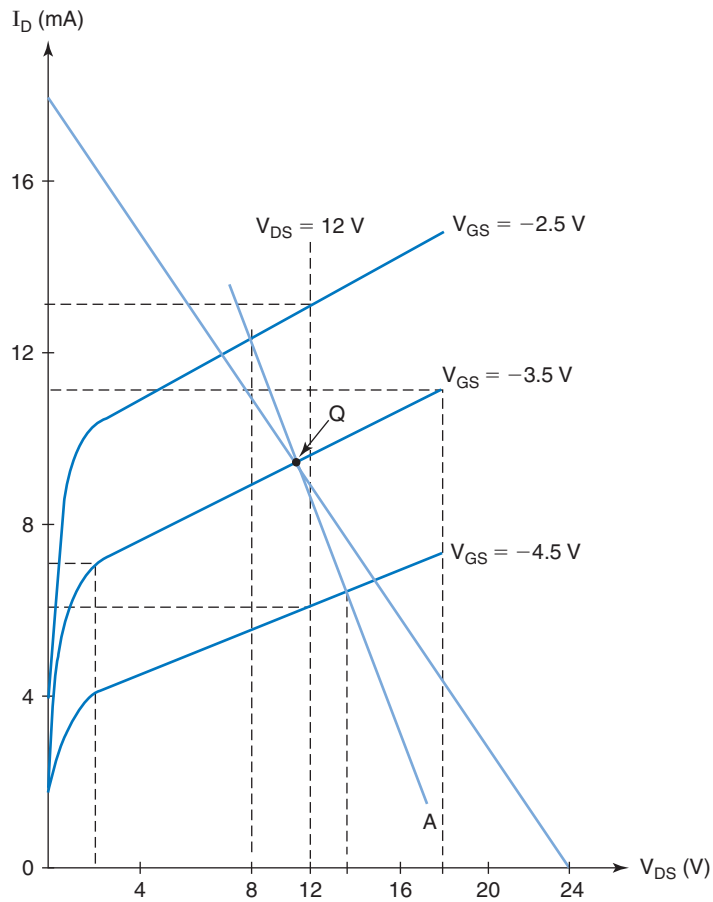


Fig. 24

- (b) Plot the d.c. load line and select a suitable Q point.
 (c) Plot the a.c. load line and determine the amplifier voltage gain when the input signal causes the gate-source voltage to vary by 2V pk-pk.

A

- (a) (i) $g_m = \frac{\delta I_D}{\delta V_{GS}}$ with $V_{DS} = 12 \text{ V}$
 and from the graphs: $\delta I_D = (13.1 - 6.2) \text{ mA} = 6.9 \text{ mA}$
 and $\delta V_{GS} = (4.5 - 2.5) \text{ V} = 2 \text{ V}$

$$g_m = \frac{6.9 \times 10^{-3}}{2}$$

$$g_m = 3.45 \text{ mS Ans}$$
- (ii) $r_{DS} = \frac{\delta V_{DS}}{\delta I_D}$ with $V_{GS} = -3.5 \text{ V}$
 $\delta V_{DS} = (18 - 2) = 16 \text{ V}$
 $\delta I_D = (11.2 - 7.2) \text{ mA} = 4 \text{ mA}$

$$r_{DS} = \frac{16}{4 \times 10^{-3}}$$

$$r_{DS} = 4 \text{ k}\Omega \text{ Ans}$$

(b) Effective a.c. load, $R_e = \frac{R_D R_L}{R_D + R_L} \text{ ohm} = \frac{1 \times 3.7}{4.7} \text{ k}\Omega$
 $R_e = 787 \Omega$ **Ans**

slope = $-1/R_e$ amp/volt = $-1/787$

slope = -1.27 mA/V (use 7.62 mA/6 V)

and the load line is plotted as shown.

$\delta V_{ds} = (13.6 - 9.2) \text{ V} = 4.4 \text{ V pk-pk}$

$\delta V_{gs} = 2 \text{ V pk-pk}$

$A_V = \frac{\delta V_{ds}}{\delta V_{gs}} = \frac{4.4}{2}$

$A_V = 2.2$ **Ans**

10 The Transistor as a Switch

The important properties of any switch are the switching time, and the ON and OFF resistances. An ideal switch would have zero ON resistance, infinite OFF resistance and take zero time to change between these two states. A mechanical switch comes very close to meeting the resistance requirements, but is slow in operation. It also has the disadvantages of comparatively large physical size and cost, and also suffers from contact 'bounce'. The latter means that as the contacts close they tend to bounce up and down rapidly before settling. This can cause major problems in digital circuits, so another solution is required. A transistor does not have zero ON resistance or infinite OFF resistance, but it is small, cheap, has a fast response time and does not have the problem of contact bounce.

A common emitter connected transistor employed as an electronic switch, together with its characteristics, is shown in Fig. 25.

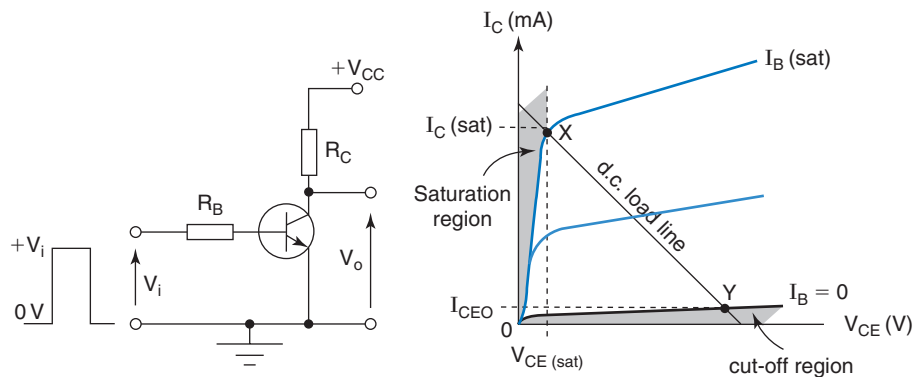


Fig. 25

For amplification purposes the transistor is operated over the linear portions of its characteristics, between points X and Y shown on the load line for R_C . For switching purposes the saturation and cut-off regions are used.

When the input voltage is at 0V then $I_B = 0$ and the transistor is said to be cut off. This corresponds to the OFF condition for the switch. In this case the circuit resistance is certainly not infinite, but will be very high since only the reverse collector current, I_{CEO} , will be flowing (a few microamps). When the input is at $+V_i$ volt the base input current will be sufficient to drive the transistor into saturation at point X, when the collector saturation current, $I_{C(sat)}$, will be flowing. This corresponds to the ON condition for the switch, and the only voltage drop across the transistor will be the small voltage (about 0.1 V) due to $V_{CE(sat)}$.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \text{ amp} \quad (6)$$

and the least value required for I_B to produce saturation, $I_{B(sat)}$, is

$$I_{B(sat)} = \frac{I_{C(sat)}}{h_{FE}} \text{ amp} \quad (7)$$

To ensure saturation the base current is arranged to be about three times the figure obtained from equation (7).

The required value for R_C may be obtained from equation (6), and the required value for R_B is obtained as follows.

$$R_B = \frac{V_i - V_{BE}}{3 \times I_{B(sat)}} \text{ ohm} \quad (8)$$

Worked Example 7

Q The transistor used in the circuit of Fig. 25 has a current gain, $h_{FE} = 90$, base-emitter voltage, $V_{BE} = 0.6\text{V}$, $V_{CE(sat)} = 0.1\text{V}$ and $I_{CE(sat)} = 4\text{mA}$. The collector supply voltage, $V_{CC} = +10\text{V}$, and the input signal level changes from 0V to $+5\text{V}$. Calculate suitable values for R_C and R_B .

A

$$I_{CE(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} \text{ amp}$$

$$\text{so, } R_C = \frac{V_{CC} - V_{CE(sat)}}{I_{CE(sat)}} \text{ ohm} = \frac{10 - 0.1}{4 \times 10^{-3}}$$

$R_C = 2.475 \text{ k}\Omega$ and the nearest preferred value is $2.2 \text{ k}\Omega$ **Ans**

Note that in this case the nearest *lower* preferred value is chosen so as to ensure saturation is achieved.

$$I_{B(sat)} = \frac{I_{CE(sat)}}{h_{FE}} \text{ amp} = \frac{4 \times 10^{-3}}{90}$$

$$I_{B(sat)} = 44.4 \mu\text{A}$$

$$R_B = \frac{V_i - V_{BE}}{3 \times I_{B(sat)}} \text{ ohm} = \frac{5 - 0.6}{133 \times 10^{-6}}$$

$$R_B = 33 \text{ k}\Omega \text{ Ans}$$

As with the common emitter amplifier circuit, inversion occurs between input and output of the transistor switch circuit shown. Thus, when the input is HIGH (saturation conditions), the output is LOW ($V_{CE(sat)} \approx 0\text{V}$), and when the input is LOW (cut-off conditions), the output is HIGH ($V_{CE} \approx V_{CC}$). If it is required for the output HIGH and LOW conditions to mimic the input conditions then the load resistor can be relocated to the emitter circuit as shown in Fig. 26. This circuit is in fact a common collector or emitter follower circuit. This name is used because the output follows the high and low states of the input.

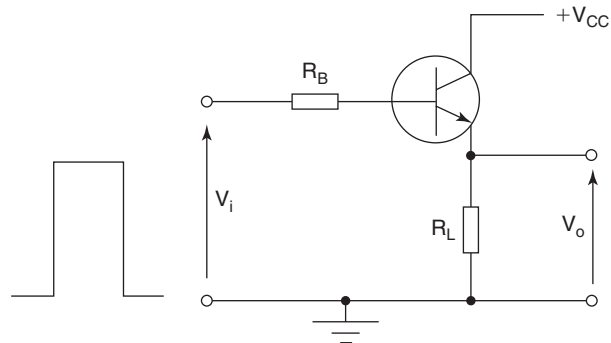


Fig. 26

If the load being supplied by the electronic switch is in the form of a power device, such as the operating coil of a relay which requires significantly higher current, then a power transistor would be employed. These can be capable of carrying currents measured in amps rather than milliamps.

A FET can also be used as an electronic switch. Being a voltage operated device it has the advantage that there is no requirement for the equivalent of R_B in the BJT circuit. The switching time for a FET is also faster than that for a BJT. For this reason FET devices are used extensively in digital switching applications, where speed of operation is paramount. On the other hand, FETs cannot handle as much power as BJTs.

Summary of Equations

Small-signal common emitter amplifier: Current gain, $A_i = \frac{\delta I_c}{\delta I_b}$

Voltage gain, $A_v = \frac{\delta V_{ce}}{\delta V_{be}}$

Power gain, $A_p = A_i \times A_v$

Small-signal FET amplifier: Voltage gain, $A_v = \frac{\delta V_{ds}}{\delta V_{gs}}$

BJT as a switch: $I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$ amp

$I_{B(sat)} = \frac{I_{C(sat)}}{h_{FE}}$ amp

$R_B = \frac{V_i - V_{BE}}{3 \times I_{B(sat)}}$ ohm

Assignment Questions

- 1 For the simply biased transistor circuit of Fig. 27, the required quiescent values for base current and base-emitter voltage are $100\ \mu\text{A}$ and 0.75V respectively. Calculate suitable values for R_B and R_C .

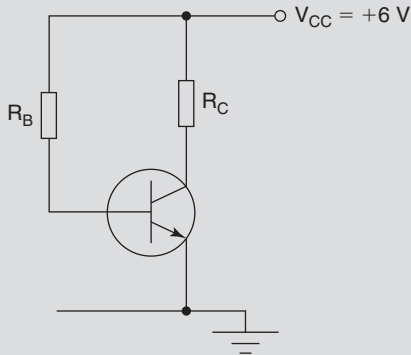


Fig. 27

- 2 The transistor in Fig. 28 has a current gain of 40 and the required bias conditions are $V_{BE} = 0.7\text{V}$ and $I_C = 2\text{mA}$. Calculate suitable values for the four resistors.

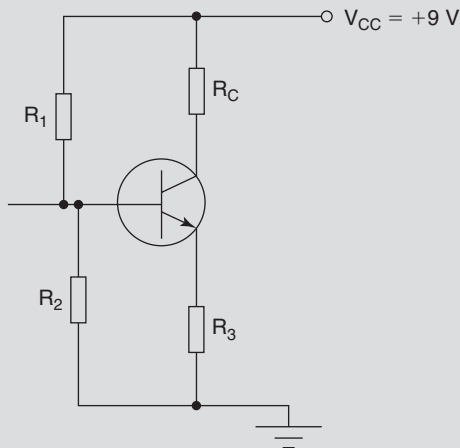


Fig. 28

- 3 The FET in Fig. 29 requires a quiescent gate-source voltage of -2V with a drain current of 5mA . Determine suitable values for R_S and R_D .

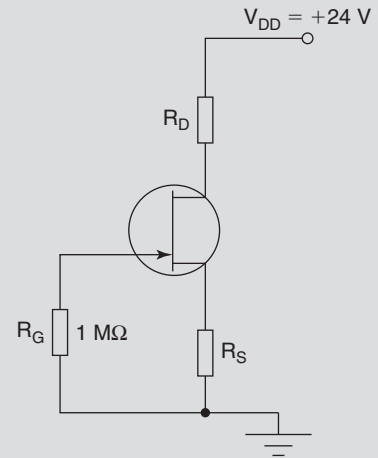


Fig. 29

- 4 The characteristics for the FET in Fig. 30 are as in Fig. 31. Using these characteristics

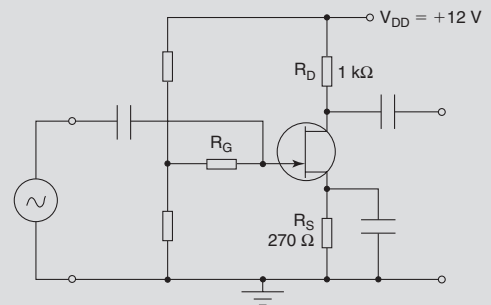


Fig. 30

- (a) Determine the mutual conductance and drain-source resistance for $V_{DS} = 6\text{V}$.
- (b) Plot the d.c. load line and hence select a suitable Q point.
- (c) Plot the a.c. load line and determine the amplifier voltage gain when the input signal causes the gate-source voltage to vary by 2V pk-pk about its quiescent value.

Assignment Questions

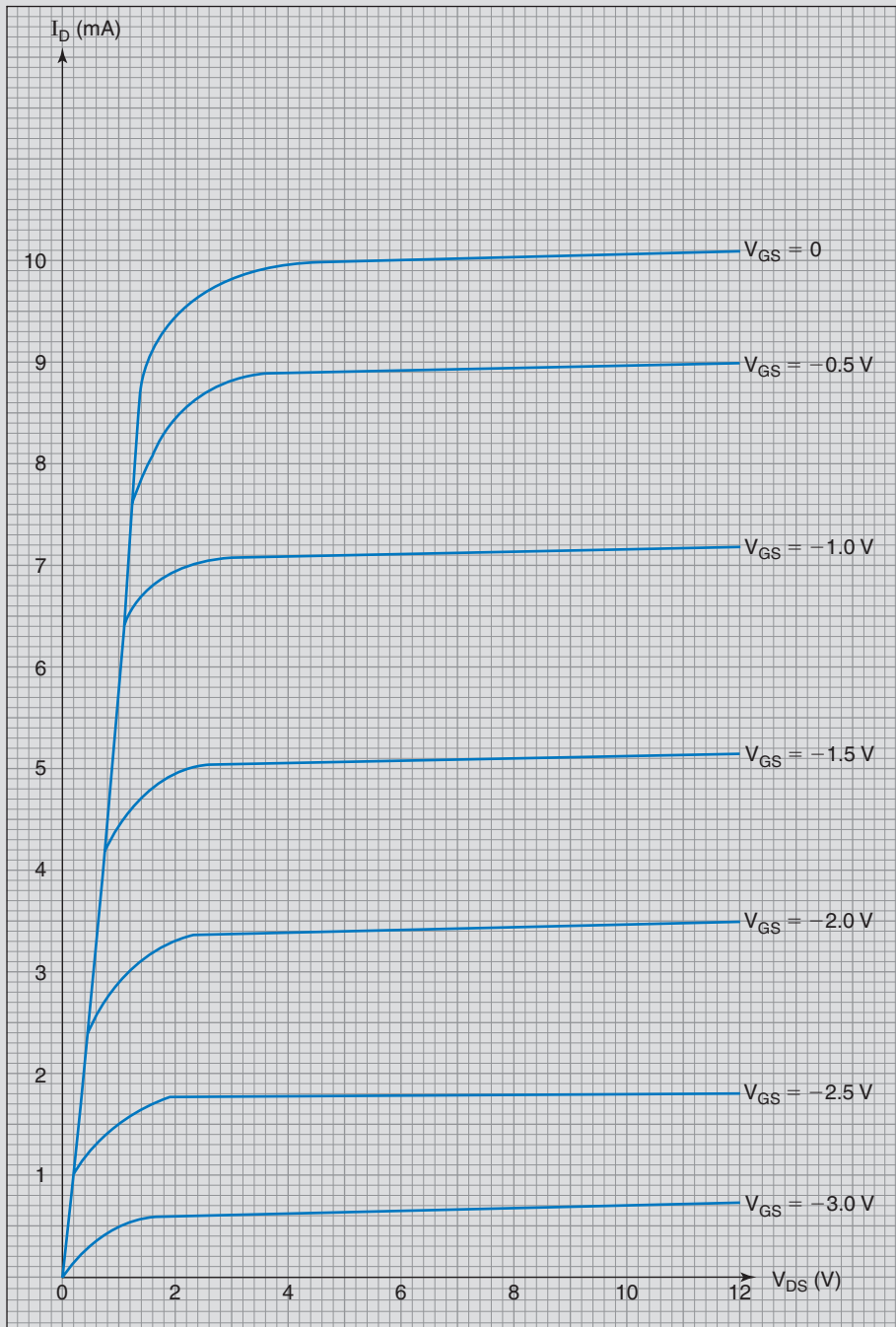


Fig. 31

Suggested Practical Assignments

Assignment 1

To investigate the use of a transistor as a switch.

Apparatus:

- 1 × general purpose BJT (e.g. a BC108)
- 1 × 10 kΩ resistor
- 1 × 100 kΩ resistor
- 1 × single pole switch
- 1 × d.c. psu
- 1 × voltmeter

Method:

- 1 Connect the circuit of Fig. 32 and set the psu output to 9V.
- 2 With the switch in position '1', note the values of V_i and V_o .

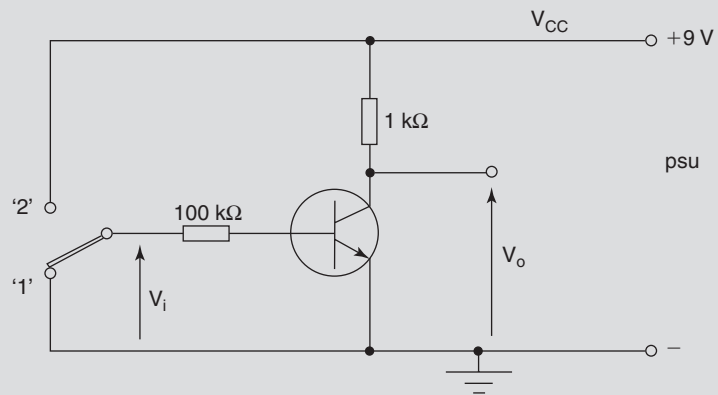


Fig. 32

- 3 Move the switch to position '2' and again note the values of V_i and V_o .
- 4 Switch off the psu.
- 5 Transfer the 1 kΩ resistor from the collector circuit into the emitter circuit, and connect the collector directly to the V_{CC} rail.
- 6 Switch on the psu and repeat steps 2 and 3 above.

Assignment 2

To investigate a small-signal BJT amplifier.

Apparatus:

- 1 × BC 108 transistor
- 4 × resistors: 4.7 kΩ, 1 kΩ, 56 kΩ, and 12 kΩ
- 1 × signal generator (and possibly an attenuator box)
- 2 × 10 μF capacitors
- 1 × 100 μF capacitor
- 1 × double-beam oscilloscope
- 1 × DVM
- 1 × d.c. psu

Method:

- 1 Connect the circuit of Fig. 33, taking care to observe the correct polarity for the electrolytic capacitors.
- 2 Set the signal generator to a sinewave output at a frequency of 5 kHz and zero volts, but do not connect to the amplifier input terminals yet.

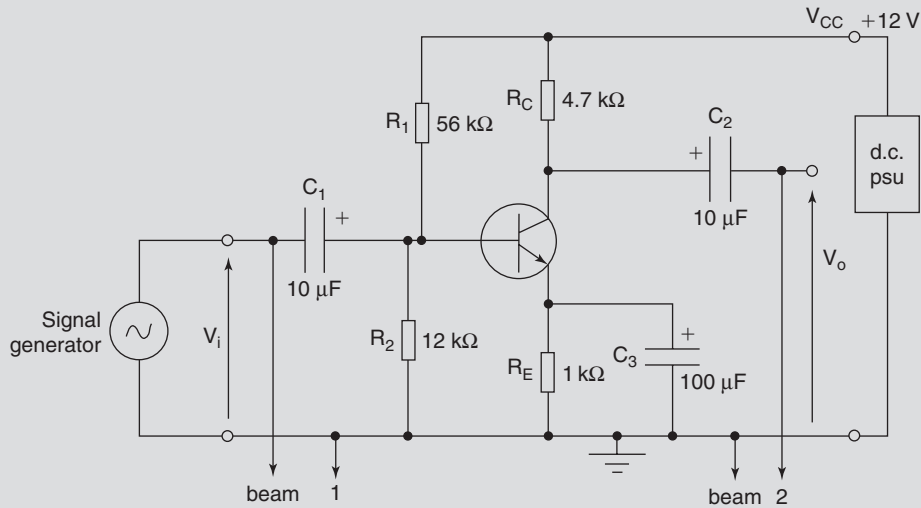


Fig. 33

- 3 Adjust the d.c. psu output to 12V.
- 4 Using the DVM measure and note the quiescent d.c. voltages listed below:
 - (a) between base and emitter;
 - (b) across R_C ;
 - (c) between collector and emitter;
 - (d) across R_E .
- 5 Connect the signal generator to the input terminals and very carefully increase its voltage so that the amplifier output voltage, V_o , is an undistorted sinewave, as shown by beam 2 of the oscilloscope. It may be necessary to connect the signal generator via an attenuator in order to provide a sufficiently small input signal to the amplifier.
- 6 Using the oscilloscope measure the amplitudes of V_i and V_o and compare their phase relationship.
- 7 Monitor the waveforms at the following points in the circuit, and by means of the DC/AC switch on the oscilloscope, determine the d.c. level about which each waveform varies:
 - (a) between base and emitter;
 - (b) between collector and emitter;
 - (c) between collector and the 0V rail;
 - (d) across R_C .
- 8 Determine the amplifier voltage gain.

Supplementary Worked Example 1

- Q** The FET used in the amplifier circuit of Fig. 34 has characteristics as given in Table 1. Using this data:
- (a) Plot the characteristics.
 - (b) Plot the load line to determine a suitable Q point and hence the corresponding quiescent values for V_{GS} , I_D and V_{DS} .
 - (c) Determine the values for R_{ds} and g_m under quiescent conditions.
 - (d) Plot the a.c. load line and hence obtain the amplifier voltage gain when V_{GS} varies about its quiescent value by 2V pk-pk.

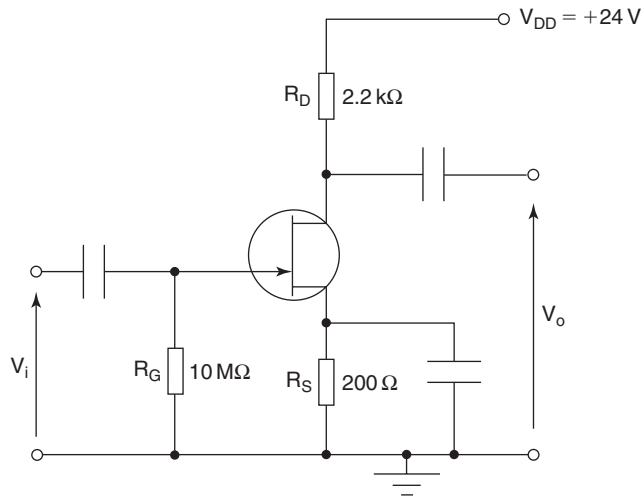


Fig. 34

Table 1

| $V_{DS}(V)$ | $I_D(mA)$ | | | | |
|-------------|------------------|------------------|------------------|------------------|------------------|
| | $V_{GS} = -2.5V$ | $V_{GS} = -2.0V$ | $V_{GS} = -1.5V$ | $V_{GS} = -1.0V$ | $V_{GS} = -0.5V$ |
| 4 | 1.4 | 2.8 | 4.4 | 6.1 | 8.0 |
| 16 | 1.6 | 3.0 | 4.6 | 6.3 | 8.2 |
| 24 | 1.8 | 3.1 | 4.7 | 6.4 | 8.4 |

A

- (a) The plotted characteristics are shown in Fig. 35.
- (b) **d.c. load line:** $V_{CC} = I_D (R_D + R_S) + V_{DS}$ volt

when $I_D = 0$; $V_{DS} = V_{CC} = 24 V \dots\dots\dots [1]$

when $V_{DS} = 0$; $I_D = \frac{V_{CC}}{R_D + R_S} \text{ ohm} = \frac{24}{2400} \dots\dots\dots [2]$

$I_D = 10 \text{ mA}$

The Q point is chosen where this load line intersects the $V_{GS} = -1.5V$ graph, and the resulting quiescent values are:

$V_{DSQ} = 13V$; $I_{DQ} = 4.58 \text{ mA}$ **Ans**

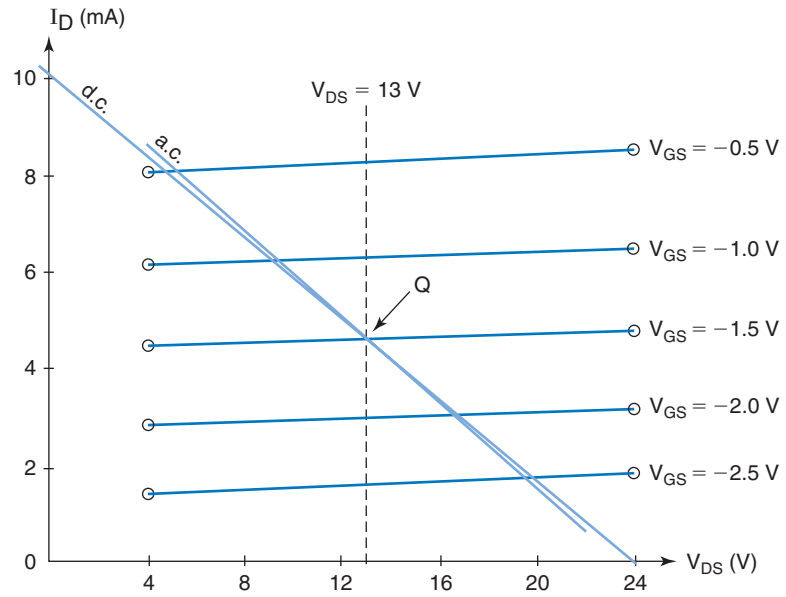


Fig. 35

(c) $R_{ds} = \frac{\delta V_{DS}}{\delta I_D}$ ohm, with $V_{GS} = -1.5$ V

$\delta V_{DS} = 24 - 4 = 20$ V; and $\delta I_D = (4.7 - 4.4)$ mA = 0.3 mA

$$R_{ds} = \frac{20}{0.3 \times 10^{-3}} \text{ ohm}$$

$R_{ds} = 66.7$ k Ω **Ans**

$g_m = \frac{\delta I_D}{\delta V_{GS}}$ siemen, with $V_{DS} = V_{DSQ} = 13$ V

$\delta V_{GS} = 2$ V pk-pk; and $\delta I_D = (8.2 - 1.6)$ mA = 6.6 mA

$$g_m = \frac{6.6 \times 10^{-3}}{2} = 3.3 \text{ mS} \text{ Ans}$$

(d) **a.c. load line:** effective a.c. load = $R_D = 2.2$ k Ω

$$\text{slope} = \frac{-1}{R_D} \text{ A/V} = \frac{-1}{2.2} \text{ mA/V}$$

slope = -0.455 mA/V (use -4.55 mA/10V), and the plotted load line is as shown on Fig. 35.

$$A_v = \frac{\delta V_{DS}}{\delta V_{GS}}$$

$\delta V_{GS} = 2$ V pk-pk; and $\delta V_{DS} = 19.6 - 5.2 = 14.4$ V pk-pk

$$A_v = \frac{14.4}{2} = 7.2 \text{ Ans}$$

Answers to Assignment Questions

- 1 $R_B = 52.5 \text{ k}\Omega$ [NPV 56 k Ω];
 $R_C = 2.5 \text{ k}\Omega$ [NPV 2.2 k Ω]
- 2 $R_E = 470 \Omega$; $R_2 = 4.7 \text{ k}\Omega$
 $R_1 = 15 \text{ k}\Omega$; $R_C = 2 \text{ k}\Omega$
[NPV 2.2 k Ω]
- 3 $R_S = 1 \text{ k}\Omega$; $R_D = 2 \text{ k}\Omega$ [NPV 2.2 k Ω]
 - (a) $g_m = 3.15 \text{ mS}$; $r_{ds} = 53 \text{ k}\Omega$
 - (b) $V_{GSQ} = -1.5 \text{ V}$; $V_{DSQ} = 5.6 \text{ V}$
 - (c) $A_V = 2.15$